



OPAL-RT

All Products Release Notes

Communication Protocols | eFPGASIM | eMEGASIM |
ePHASORSIM | RT-LAB | RT-XSG | MMC | Schematic Editor

Latest Update: July 30, 2020



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Version 2020.2.2

Features

- MIL-STD-1553: Improved mechanism used for the automatic enabling of the 'Data ready' signal

Bugfixes

- DNP3 Slave: Fixed issues with configurations containing many signals
- IEC61850: Fixed crash when inputting incompatible SCL files (in the context of GOOSE and SV NLE lists)
- OP4200: Fixed issue with programmed timestep value in the FPGA
- SCPI: Fixed issue of the driver blocking the load of the model when the destination IP cannot be reached
- CAN: Fixed channel indexing issue
- CAN: Fixed problems arising with configurations having a large number of messages (10,000+)

Version 2020.2.1

Features

- RT-LAB: Software synchronized has been improved on Windows simulation to support model timestep below 1ms.

Bugfixes

- RT-LAB: Fixed call to SetParametersByName(), was generating overrun.
- RT-LAB: Fixed time used to initialize OpalBoard Driver when loading a model.
- RT-LAB: Fixed version of Python set up on OP6000 target.
- CAN: Fixed issue with the model not receiving CAN messages (DRVTT-1142)
- DIANE: Fixed indexing of arrays starting at 0 (DRVTT-1167)
- AFDX: Fixed validation of ES and VL IDs (DRVTT-1158)
- AFDX: Improved path filtering when inputting a .hex or .adc file (DRVTT-1157)
- SCPI: Fixed automatic command formatting for MAGNA power supplies (DRVTT-1174)
- Fast Scope FPGA: Fixed issue preventing the FPGA scope from being enabled (PJ000244-171)

Version 2020.2.0

Features

- RT-LAB: Improved robustness of RT-LAB's configuration panel.
- RT-LAB: The license server cannot be started twice on the same server.
- RT-LAB: Blocked MATLAB (32 bits) when using a 64-bit compiler to avoid undefined behavior.
- RT-LAB: New RT-LAB Python API method "InstallRtlab" available to install RT-LAB on a target.
- RT-LAB: New RT-LAB Python API method "UninstallRtlab" available to uninstall RT-LAB from a target.
- RT-LAB: Improved compilation time when using MingW.

- RT-LAB: Added documentation on MingW compiler.
- RT-LAB: Updated example model in .slx and latest MATLAB versions supported.
- RT-LAB: Checked validity of path given in parameter of "CreatePackage" method available through RT-LAB's Python API.
- RT-LAB: Updated RT-LAB's Python API documentation with ImportConnections, ExportConnections, CreateConnection and DeleteConnection methods.
- RT-LAB: "Force Refresh" button available through right-clicking a connection in the RT-LAB configuration panel is moved to the toolbar of this panel.
- RT-LAB: Added check on disk space available when installing RT-LAB on a target.
- RT-LAB: DataLogger Python API now supports Python 3.7. Python version 2.2, 2.3, 2.4, and 2.5 are no longer supported.
- RT-LAB: ScopeView: Added documentation related to OPACQ (Choosing Data Logger as a Data Source).
- RT-LAB: ScopeView: Added trigger position and acquisition period parameters for Data Logger acquisitions.
- ePHASORSIM: New version for Excel template (V1.8): add service status as an input parameter for Loads, Lines and Transformers in both positive sequence and multi-phase libraries (EP-1718).
- ePHASORSIM: Be advised that V1.6 and V1.7 will be discontinued in the next release.
- ePHASORSIM: For PSS/e input files and built-in library, from RAW file now it also imports all supported components whose status is '0'. In case of incorporating FMUs, the initial status of corresponding component in the RAW file must be '1', otherwise the data will not be imported.
- ePHASORSIM: Enable Power-flow to incorporate status of native components in to its calculations (EP-1677).
- ePHASORSIM: Two protection relay models are added to Simulink library: generic over-current and out-of-step.
- ePHASORSIM: A new example (PHASOR-02) to simulate cascading outage is added that uses new Simulink Based Protection Relays (EP-1726).
- ePHASORSIM: In Modelica library a new parameter called 'partType' is added. See user-guide for more details (EP-1707).
- ePHASORSIM: Updated and revised the user guide (EP-1744).

- EtherCAT Slave: Added support for using multiple cards in one simulator (DRV-3456)
- MIL-STD-1553: Added support for error injection for remote terminals (DRV-3463)
- OPAL-RT Board: Added support for MMC for central systems (DRV-3223)
- AFDX: Added new Sfunction driver for AFDX (Arinc 664P7) communication (DRV-3279)
- FPGA Scope: Added functionality for intra-step FPGA signal monitoring with ScopeView (PJ000244-3)
- PICKERING: Added support for GUI configuration (DRV-3436)
- PICKERING: Added support for all Opal-RT-supported cards into one interface (DRV-3437, DRV-3438)
- OPC-UA Server: Added support for GUI configuration (DRV-3393)
- SCPI: Added connection points for easier debugging (DRV-3345)

Bugfixes

- RT-LAB: IO entries are no longer duplicated in the project tree explorer
- RT-LAB: Pre-trigger percentage is ignored if the value starts at 0.
- RT-LAB: Fixed "Time Factor" parameter when simulating on the localhost.
- RT-LAB: License validation no longer reporting erroneously when used for multiple hosts.
- RT-LAB: Getting a frame from Datalogger in a second run no longer fails.
- RT-LAB: Fixed error loading a model on an inaccessible target.
- RT-LAB: Frame configuration of Datalogger through the Python API, when using a value higher than a 32 bits value, now works.
- RT-LAB: MetaController presence is now detected at boot of RT-LAB.
- RT-LAB: Orchestra example models are now compilable with the MingW compiler.
- RT-LAB: Logs now displayed correctly when loading a model.

- RT-LAB: Slowness fixed when displaying windows containing project examples.
- RT-LAB: "Disconnect selected" option, available in RT-LAB configuration panel, now fixed.
- RT-LAB: "Open with ScopeView" button, available through a right-click on a SignalGroup, now fixed.
- RT-LAB: Print displayed by SyncExchanger tool now fixed.
- RT-LAB: Embedded mode now fixed.
- RT-LAB: "Simulation Tools" entry in RT-LAB Preferences now fixed.
- RT-LAB: Removed extra separator in the Connections menu, in the RT-LAB configuration panel.
- RT-LAB: Fixed email address of the Support team displayed when requesting a new license fails.
- RT-LAB: Web service for requesting licenses is now available.
- RT-LAB: RT-LAB asking to set up a target already set up is fixed.
- RT-LAB: Renamed "Assigination" Tab in model view "Assignment" Tab.
- RT-LAB: Recorder now visible in project tree explorer.
- RT-LAB: Fixed the use of vectors with Orchestra.
- RT-LAB: Fixed OPREC file generation when no signals are present or when checked in a signal group.
- RT-LAB: Fixed project creation when nothing is selected.
- RT-LAB: Fixed model compilation detection, when compiled with an older version of RT-LAB.
- RT-LAB: Fixed pop-up message "RT-LAB already installed on the target" when loading a model on a target that is correctly set up.
- RT-LAB: Fixed options available when creating a new project.
- RT-LAB: Fixed Monitoring Tab when using a Multi-target system based on Dolphin.
- RT-LAB: Fixed OpInput block shown in project tree explorer when using a MATLAB environment variable for the default value.
- RT-LAB: Fixed RT-LAB installation.

- RT-LAB: Fixed error "Could not get the logical node ID" when trying to load a model.
- RT-LAB: Fixed error "File not found: path_to_subsystem/subsystem_name.map" when compiling a model.
- RT-LAB: Fixed error "Did not receive status from some nodes" when loading a model.
- RT-LAB: Removed erroneous text from the "Probe Control" panel.
- RT-LAB: Fixed count of connections selected when removing them from RT-LAB's configuration panel.
- RT-LAB: Fixed target status.
- RT-LAB: ScopeView: Fixed navigation in the OPREC file.
- CAN: Fix for CAN IDs greater than 29 bits (DRVTT-1118)
- CAN: Fixed stability issues (DRVTT-1091, DRVTT-1106)
- OPAL-RT Board: Fixed issues when fetching bitstream files from the standard repositories (DRVTT-1121)
- IEC61850: Corrected driver to send the data types as defined in the .icd file for SV NLE (DRV-3392)
- IEC61850: Removed interface pre-configuration when adding it to a project (DRVTT-42)
- IEC61850: Fix for malformed SV packets when svID or data uses more than 128 octets (DRVTT-1057)
- SCPI: Improved user interface (DRVTT-1043)
- SCPI: Fixed driver when used with a Magna Power Source (DRV-3367)
- PICKERING: Ignore notion of bits per channel for resistive cards not using the precision setting (DRV-3425)
- MODBUS: Fixed issues appearing due to error codes 32 and 9 (DRVTT-1079)
- Synchronization: Changed the network interface selection to be a text field (DRV-3363)

Version 2020.1.0

Features

- RT-LAB : Support included for MATLAB R2019 a/b. (Note that MATLAB R2019b is no longer supported on Windows 7.)
- RT-LAB : Added autoconnection feature in the project configuration view. (see RT-LAB Help for more details.)
- RT-LAB : Added a DataViewer button in the main RT-LAB toolbar, adjacent to the ScopeView icon
- RT-LAB : Support of floating licenses for the RT-LAB and ARTEMIS core(s)
- RT-LAB : Improved responsiveness for opening projects containing more than 10,000 aliases and IO connections
- RT-LAB : Added an internal logger to the RT-LAB interface
- RT-LAB : Added support for 4 ASM cards on the OP6000
- RT-LAB : Decommissioned MATLAB versions below R2015b.
- RT-LAB : Provided Orchestra dynamic library for co-simulation
- RT-LAB : Re-introduced the web service where license encryptions are sent to Support (and updated the address to contact in case of error)
- RT-LAB : Removed the Orchestra Dymola block from the block library
- RT-LAB : ScopeView: Added ability to load OPACQ sources after Open with ScopeView actions
- RT-LAB : ScopeView: Improved the reconnection to OPACQ sources between two runs
- RT-LAB : ScopeView: Trigger parameters are now grayed-out if no trigger is detected
- RT-LAB : ScopeView: Fixed incorrect trigger configuration after a reconnection
- RT-LAB : Support of Mingw compiler for Windows model
- RT-LAB : Changed Number of CPUs to Number of Cores when displaying target details
- RT-LAB : Updated example model for MATLAB 2015b, with .slx format

- RT-LAB : Update LabVIEW API example to be compatible with the supported versions of LabVIEW(> 2012)
- RT-LAB : Updated RT-LAB user documentation
- RT-LAB : Updated RT-LAB user online Help
- OPAL-RT Board: Added support for TSBIn (Digital In Average) (DRV-3244)
- OPAL-RT Board: Added support for PWM synchronized AIN (DRV-3243)
- OPAL-RT Board: Added support for .opbin bitstream description file (DRV-3270)
- OPAL-RT Board: Improve mechanism of how .opal/.bin/.opbin files are handled (DRV-3294)
- OPAL-RT Board: Add support for the OP5334 card (DRV-3265 and DRV-3266)
- C37.118 master: Add option to configure local UDP port (DRV-3318)
- CAN: Add option to dynamically control the cyclic rate of transmitted messages (DRV-3261)
- PICKERING: Added support for 50-298-020 and 50-110A-021 cards (DRV-3323 and DRV-3324)
- ePHASORSIM: New design for mask of Solver block (EP-693).
- ePHASORSIM: All the Excel files with versions lower than V1.6 has been discarded. Be advised that V1.6 and V1.7 will be discontinued in the next release.
- ePHASORSIM: New feature to replace FMUs by native library exclusively in case of PSS/e input files.
- ePHASORSIM: Throw error for inconsistency in licence keys (EPTT-113).
- ePHASORSIM: Addition of description for HVDC parameters in PHASOR-11 (EPTT-42).
- ePHASORSIM: Updated and revised the user guide (EP-1640).
- ePHASORSIM: Dropped the support of Matlab versions lower than R2015b (EPTT-112).

Bugfixes

- RT-LAB: Working sets should no longer disappear randomly
- RT-LAB: CAN: multiple connections now appear for one block
- RT-LAB: Fixed number of connections displaying in the configuration view of RT-LAB when trying to disconnect the selection
- RT-LAB: Improved performance of the DataViewer to support more than 3,000 signals per signal group
- RT-LAB: Improved performance of load/reset project where it contains LabVIEW panels
- RT-LAB: Improved Stop function of DataLogger Tool to avoid generating zombie processes on the target
- RT-LAB: IO no longer duplicated after opening a project
- RT-LAB: Enhanced the robustness of close project
- RT-LAB: Made RT-LAB 2020.1 and up compatible with eHS Gen3 x64 or eHS Gen3 x128
- RT-LAB: Offline mode on OpWriteFile block has been fixed
- RT-LAB: Removed info.xml file from the toolbox for MATLAB R2013b
- RT-LAB: Values returned by getSignalsByName are now in the correct order
- ePHASORSIM: Resolve the conflicts in the name of functions in common with matlab, deg2rad and rad2deg (EPTT-145).
- OPAL-RT Board: Fix default values of AO signals (DRVTT-1046)
- OPAL-RT Board: Fix for how synchronization types work (DRVTT-1035)
- OPAL-RT Board: Fix for initial phase not working when 'Complementary Output' is checked (DRVTT-940)
- IEC61850: Fix import of projects created on a different host (DRVTT-934)
- IEC 61850: Improved ICD file parsing when element names are duplicated (DRVTT-891)
- IEC 61850: Fixed validation of uniqueness of GOOSE messages done using the MAC address in combination with the AppID (DRVTT-942)

- ARINC429: Fix issue with BNR data resolution
- Modbus: Fix loading of slave driver in RTU mode on the OP4200 (DRVTT-991)
- DNP3: Fix issue with negative values transmitted or received (DRVTT-865)
- CAN: Change the way received CAN frames are stored in memory so that data accuracy is not lost (DRVTT-1037)
- CAN: Provide a way to swap the gain/offset calculation (DRV-3262)

Version 2019.3.2

Features

- PICKERING: Added support for 50-297-041 and 40-298-050 resistive cards (DRV-3085)

Bugfixes

- RT-LAB: No longer changes the Python default version present on the target with RedHat 32bit LINUX. 2.4 is maintained for the system and 2.7 for scripting.

Version 2019.3.1

Features

- DIANE: Added new IO interface for DIANE Ethernet-based communication protocol (DRV-3176)

Bugfixes

- ARINC-429: Fixed issue with transmission when the embedded recording feature was used (DRVTT-998)

Version 2019.3.0

Features

- RT-LAB: Support for Windows 64-bit
- RT-LAB: Improved performance of connection creation
- RT-LAB: Improved license management for ARTEMIS, based on cores
- RT-LAB: Improved opening/closing of RT-LAB and projects
- RT-LAB: Improved post-trigger treatment in ScopeView
- RT-LAB: LabVIEW: Improved time to load and reset a model with panels open
- RT-LAB: License is now based on END_OF_SUPPORT_DATE
- RT-LAB: Optimized compilation time of Orchestra framework
- RT-LAB: Python: Default version setup by RT-LAB is 2.7 (Host and Target)
- RT-LAB: Python: RT-LAB API now supports Python 3.7
- RT-LAB: Python: Versions 2.2 to 2.5 no longer supported
- RT-LAB: Recorder: Added documentation for json configuration file for the DataViewer
- RT-LAB: Recorder: Added internal timing
- RT-LAB: Recorder: Users can now increase the DataLoggerTool priority
- RT-LAB: Recorder: Users can now select SignalGroups in the DataViewer

- RT-LAB: RT-LAB API: Added a function to get datapoints on I/O (getConnectionPointsForIO)
- RT-LAB: RT-LAB API: Added a function to get the list of I/O available (getIOInterfaces)
- RT-LAB: RT-LAB API: Import connections function doesn't stop if the creation of a connection fails
- RT-LAB: RT-LAB API: Added support of linked models when using CreatePackage function
- ePHASORSIM: New native components: GENSAL, GENSAE, ESAC1A, ESAC5A, ESAC6A, ESDC1A, ESDC2A, ESST1A, ESST4B, EXAC1, EXAC2, EXDC2, EXPIC1, IEEET1, IEEEX1, IVOEX, SCRX, URST5T, IEE2ST, IEEEST, PSS2A, PSS2B, GAST, HYGOV, IEESGO, CRANIT (exclusively for PSS/e dyr input file)
- ePHASORSIM: A new example with CRANIT based on Kundur's two-area system is added (PHASOR-24)
- ePHASORSIM: Optimizations in the run-time performance up to 30%
- ePHASORSIM: Extensive warning messages are added to prevent of using invalid dynamic parameters. These messages are visible via "Diagnostic Viewer" in Simulink file
- TCP/UDP: Added new IO interface for TCP/UDP communication (DRV-3106)
- OPAL-RT Board: Added support for distributing connections onto multiple subsystems (DRV-3061)
- OPAL-RT Board: Added support for OP4510 chassis using a TE0741 410T FPGA (DRV-3059)
- CAN: Added support for ARXML DB files (DRV-3138)
- CAN: Added option to enable/disable a channel (DRV-3171)

Bugfixes

- RT-LAB: Bug fix on aliases (refresh and creation)
- RT-LAB: Bug fix on DisconnectAll in configuration view
- RT-LAB: RT-LAB API: Bug fix on export connections function

- RT-LAB: RT-LAB API: Bug fix on import connections with ~3000 connections
- RT-LAB: Bug fix on RT-LAB uninstall from 64 bit targets
- RT-LAB: Bug fix on VariableTable and WorkingSets (refresh and signals assignation through drag and drop)
- RT-LAB: Bug fix related to use of OpWriteFile ("daemon is busy")
- RT-LAB: Changed Serial Number images for licenses
- RT-LAB: LabVIEW: Bug fix on connections not loaded in panels
- RT-LAB: LabVIEW: Bug fix on connections only available after a close/open of the project in the configuration view
- RT-LAB: LabVIEW: Bug fix when re-opening panels after a close/open of RT-LAB or the project
- RT-LAB: LabVIEW: Bug fix when saving and closing panels
- RT-LAB: Recorder: Bug fix memory leak
- RT-LAB: Recorder: Bug fix on deleting a recorder
- RT-LAB: Recorder: Bug fix on icons displayed in the UI (red circle/blue square)
- RT-LAB: Recorder: Bug fix on trigger value and holdoff parameter
- RT-LAB: ScopeView: Bug fix on frame, conversion from steps into seconds
- RT-LAB: ScopeView: Bug fix on live acquisition with a length upper than 4 seconds
- RT-LAB: ScopeView: Bug fix on splash screen
- RT-LAB: ScopeView: Bug fix to have scope unit into seconds
- ePHASORSIM: For OpenModelica based FMU's a 32bit compiler (in RT-LAB/Development/Compiler tab) must be chosen when localhost is the simulation target.
- CAN: Fixed issue when importing a signal that has Motorola endianness (DRV-3163)
- C37.118: Fix issue of fraction of a second not properly rounded (DRVTT-897)
- Modbus: Ensure that the driver binds on the network interface specified in the configuration (DRVTT-894)
- VC707 Sfunction driver: Fix voltage range issue for group 3B of the OP5607 chassis (DRVTT-914)

- OPAL-RT Board: Improve search for bitstream binary file (DRVTT-933, DRVTT-904)
- OPAL-RT Board: Fix support for Encoder functionality on remote systems (DRVTT-921)
- OPAL-RT Board: Keep the configuration of the synchronization cable when switching between master and slave modes (DRVTT-887)
- OPAL-RT Board: Fix synchronization issues with MuSE simulations running on OPAL-RT Linux (x64-based) platforms (DRVTT-905)
- ARINC429: Fix issue of JSON configuration file modification not detected (DRVTT-925)

Version 2019.2.5

Bugfixes

- RT-LAB: Fix Matlab compilation issue, stuck at 20%.

Version 2019.2.4

Bugfixes

- ARINC-429: Improvement of mechanism that determines if data should be read from the card.

Version 2019.2.3

Bugfixes

- RT-LAB/DataLogger: Remove a signals from a SignalGroup in RTLAB doesn't remove it.

Version 2019.2.2

Features

- RT-LAB: MetaController has an option to start in console mode.

Version 2019.2.1

Features

- SCPI: Added support for the Keysight RP79xx device family along with support for generic SCPI devices (DRV-3040)
- MIL-STD-1553: Added an option to automatically enable the 'data ready' signal of RT send blocks when new data is available (DRV-3055)
- MIL-STD-1553: Increased the number of options in the RT receive blocks for the size of the firmware queue dealing with interrupts (DRV-3049)
- CAN: Added support for automatic data logging and signal visualization (DRV-3050)
- CAN: Added support for the Vector__XXX node (DRVTT-844)
- ARINC-429: Added extra data logging parameters (output file-naming, append timestamp to filename, frame length units, export format, triggering) (DRV-3035)
- ARINC-429: Updated example project to contain DataViewer example table configuration (DRV-3035)
- Driver DataViewerAPI: Added Python API to create the table configuration (DRV-3066)

Bugfixes

- RT-LAB/DataLogger: Fix in DataView (RTLABTT-2293)
- RT-LAB: fix memory leak in orchestra API (RTLABTT-2293)
- RT-LAB: Method RTGetInstance_Id remove from orchestra API, and replace by script get_instance.py (RTLAB-2682)
- C37.118 master: Fixed problem when master was started before PMU (slave) (DRV-3068)
- C37.118 master: Fixed problem when the PMU (slave) sent its configuration not aligned to the next second (DRV-3068)
- Modbus master: Fixed problem of disconnection and reconnection occurring on any communication error with the slave (DRVTT-842)
- Modbus master: Fixed load problem on OP4200 for RTU mode (DRVTT-828)

Version 2019.2

Features

- RT-LAB: Added possibility to create and deploy multiple instances of a same project (RTLAB-2589)
- RT-LAB: Performance optimization for OpInput and OpOutput blocks (RTLABTT-2050)
- RT-LAB/Orchestra: Input pin of Orchestra_Proxy_C and Orchestra_Proxy_Simulink block added to control when to unblock an Orchestra client (RTLABTT-1705)
- RT-LAB/DataLogger: "Log File Length" parameter is now replaced by "Number of Frames" (RTLAB-2588)
- RT-LAB/DataLogger: Added absolute timestamp in metadata. (RTLABTT-1629)
- RT-LAB/API DataLogger: Added getLastValues() function in the API (RTLAB-2616)
- Modbus slave: Added support of the new configuration interface (DRV-3001)
- Modbus master: Added support of 32-bit floating point values (DRV-1865)

- OPAL-RT Boards: Added support of of OP7000v2 system (OP7000NG-270)
- ARINC-429: Added beta support for automatic data logging and signal visualization (DRV-3035)
- Ethernet drivers: Replace the drop down list to select the network interface by an editable field (DRV-2992)
- CAN: Added option to monitor the load of the bus (DRV-2810)
- ePHASORSIM: New native components: EXPIC1, ESAC5A, EXAC2, SCRX, IEEE1, IEEE2, IEEE3, HYGOV, GAST models (exclusively for PSS/e dyr input file)
- ePHASORSIM: License update is required (2019.2)

Bugfixes

- RT-LAB: Fixed ImportConnections() function issue when the project has multiple subsystems (RTLABTT-2121)
- RT-LAB/DataLogger: Fixed Decimation Factor issue (RTLABTT-2138)
- RT-LAB/DINAMO: Fixed Nelder-Mead algorithm (RTLAB-2587)
- C37.118 slave: Fixed problem with streaming rate when many slaves were configured (DRVTT-776)
- OPC-UA server: Fixed problem when more than 50 data points were configured (DRVTT-814)
- MIL-STD-1553: Fixed issue that was preventing to receive all messages when the rate was faster than the model step (DRVTT-719)
- Modbus master: Fix load error in RTU mode when the configured serial interface is not existing (DRVTT-778)

Deprecation and Removals

- RT-LAB/Orchestra: Remove Dymola proxy bloc and Dymola Client Example (RTLAB-2624)

Version 2019.1

Features

- RT-LAB: New RT-LAB versioning scheme (year.release_number) for better consistency, predictability and transparency
- RT-LAB: Added Compatibility with MATLAB R2018a and MATLAB R2018b
- RT-LAB/DataLogger: Added option to convert a recorded file between .oprec, .csv and .mat (RTLAB-2114, RTLAB-2365)
- OPAL-RT Boards: Added support of automatic firmware reprogramming (DRV-2565)
- OPAL-RT Boards: Added an option to disable the strict hardware mismatch validation (DRV-2911)
- OPAL-RT Boards: Added support of 64 data inputs/data outputs ports (DRV-2914)
- ARINC-429: Added embedded data logging option to record signals on each channel of the Abaco card (DRV-2905)
- ARINC-429: Added support of multiple BNR signals into the same message (DRV-2838)
- ARINC-429: Added support of multiple imports of a configuration file (DRV-2869)
- ePHASORSIM: Interdependency between synchronous machines and their controllers is not a limitation anymore
- ePHASORSIM: Beta release for native components: GENROE, EXAC4, SEXS, STAB3, STAB4, IEEEG2 models (exclusively for PSS/e dyr input file)
- ePHASORSIM: New version of Excel template (V1.7): EX_T1, PSS_T1 and TG_T1 are deprecated
- ePHASORSIM: A new example with Simulink based switched shunt controller is added (PHASOR-23)
- ePHASORSIM: License update is required (2019.1)

Bugfixes

- RT-LAB: Fixed Model Referencing compatibility with MATLAB R2016a, R2017b, 2018a and 2018b (RTLABTT-227, RTLABTT-1417)
- RT-LAB: Fixed display of Identifier parameter in OpInput and OpOutput blocks (RTLABTT-901)
- RT-LAB: Fixed Datalogger and Connections issues after renaming a subsystem (RTLABTT-1348, RTLABTT-1365)
- RT-LAB: Fixed LabVIEW panel Connections with console lost after RT-LAB restart (RTLABTT-1673)
- RT-LAB/DataLogger: Fixed issue when trying to delete signal group from the Recorders hierarchy (RTLABTT-1340)
- RT-LAB/DataLogger: Fixed Pre-trigger percentage functionality (RTLABTT-1524)
- ARINC-429: Fixed issue with multiple send blocks on Max Technologies solution (DRVTT-702)
- IEC61850: Fixed publishing/subscribing of a basic data attribute within a GOOSE message (DRVTT-734)
- IEC61850: Fixed GOOSE subscriber losing packets upon a publisher stop/start sequence (DRVTT-735)
- C37.118 master: Added a connection point to flag mismatch between master and slave configuration (DRVTT-730)
- ePHASORSIM: FMUCreator gets the Linux target credentials (EPTT-84, 91)

Version 11.3.6

Features

- RT-LAB: Removes Visual Studio Code packaging into the product. VSCode can still be used as part of a separate download

Bugfixes

- RT-LAB: Fixed RTE signal library to improve reliability for MATLAB R2016b and later (SOLVTT-159)
- MIL-STD-1553: Fixed unexpected traffic on RT0/SA0 (DRV-2866)
- Modbus master: Fixed naming issue when duplicating a slave (DRV-2879)
- IEC60870-5-104 slave: Fixed naming issue when duplicating a slave (DRV-2878)
- DNP3 master: Fixed naming issue when duplicating a slave (DRV-2892)

Version 11.3.5

Features

- OPAL-RT Boards: Added support of analog outputs multirange for remote systems (DRV-2850)
- DNP3 slave: Added option to migrate the communication on a dedicated CPU core(DRV-2880)
- RT-LAB/DataLogger: Added DataLogger Python script example (RTLABTT-1390)
- RT-LAB/DataLogger: Added error reporting messages in DataLogger Python API (RTLABTT-1382)
- RT-LAB/DataLogger: Added method to get the recording status in the Python API (RTLABTT-2320)

Bugfixes

- OPAL-RT Boards: Fixed model execution on OP4200 platform (IOSFP-618)

- OPAL-RT Boards: Fixed reset issue when a wrong board index is specified in the configuration (IOSFP-618)
- RT-LAB: Fixed rc.local update when installing a new RT-LAB version (RTLABTT-1452)
- RT-LAB/API: Fixed New Python API to read OPREC file correctly (RTLABTT-1441)
- RT-LAB/LabVIEW panel: Fixed special characters management in LabVIEW panels for RT-LAB (RTLABTT-1279)
- RT-LAB/LabVIEW panel: Fixed connection loss on parameters/signals (RTLABTT-1230)
- RT-LAB/DataLogger: Fixed recording file creation when recorder mode is set to "Manual" (RTLABTT-1420)
- RT-LAB/DataLogger: Fixed duplicated OPREC output files (RTLABTT-1401)
- RT-LAB/DataLogger: Fixed RT-LAB freezes when datalogging over 1200 signals (RTLABTT-1392)
- RT-LAB/DataLogger: Fixed ordering of elements in vector signals (RTLABTT-1387)
- RT-LAB/DataLogger: Fixed Crash Controller from DataLogger example model (RTLABTT-1389)
- RT-LAB/DataLogger: Fixed DataLogging console crashes with multi-models projects (RTLABTT-1344)
- RT-LAB/DataLogger: Fixed RT-LAB freeze due to DataLogger config (RTLABTT-1411)
- RT-LAB/DataLogger: Fixed timestamps reorganization in .OPREC and .CSV recorded files (RTLABTT-1412)
- RT-LAB/DataLogger: Fixed signal assignation from one subsystem on a recorder of another subsystem (RTLABTT-1458)
- RT-LAB/DataLogger: Fixed RT-LAB temporary freeze after the first click on a signal group (RTLABTT-1507)
- RT-LAB/DataLogger: Updated API naming (RTLAB-2414)

Version 11.3.4

Features

- Introducing OPAL-RT Schematic Editor: Design, configure and integrate electrical circuit simulation on OP5707 and OP4510 using eHS
- eHS: Enhance usability by supporting OPAL-RT Schematic Editor circuit
- eHS: Enhance usability by managing parameter configurations on the schematic
- RT-LAB/DataLogger: Now possible to manually start and stop recordings while the simulation is running (RTLAB-2118)
- RT-LAB: Support for MATLAB R2017b (RTLAB-1984)
- RT-LAB: "OPAL-RT Board" I/O interface can now be associated to a slave subsystem (RTLABTT-1293 and RTLABTT-965)
- RT-LAB/DINAMO: Added a quadcopter example model with integration for DINAMO and X-Plane. (RTLAB-2244)
- RT-LAB/API: Execute and Load API functions now accept a -1.0 time factor value. This will use the previously defined time factor value (RTLABTT-1285)
- RT-LAB/API: New GetConnectionsDescription API function for accessing connection information (RTLABTT-1266)
- RT-LAB/API: New ImportConnections and ExportConnections API functions (Python only) (RTLAB-2338)
- RT-LAB/Orchestra: Added "File version" to OpalOrchestra.dll, OpalOrchestra_64.dll, and OpalOrchestraVISA.dll (RTLABTT-1328)
- Added support of Resolver inputs and Resolver outputs on OP4200 system (DRV-2652)
- OPAL-RT Boards: Added support of OP5650 (Artix 7) platform, including MuSE (DRV-2564)
- OPAL-RT Boards: Added support of analog outputs multirange (central systems and OP4200 only) (DRV-2851)
- MuSE: Added support of synchronization through the SFP cable (IOSFP-588)
- MuSE: Fixed issue with central system that had to reload a user bitstream to perform the enumeration (DRVTT-618)
- MuSE: Improved global stability of remote bitstream reprogramming (DRVTT-610)

- ePHASORSIM: Support Dymola (Ver. 2019) to create FMU (requires license key EPHASOR_DYMOLA_FMU)
- ePHASORSIM: Support MATLAB 64-bit (R2016b, R2017a)
- ePHASORSIM: License update is required (2018.1)
- ePHASORSIM: Example PHASOR-11 has a new HVDC model

Bugfixes

- RT-LAB/DataLogger: Fixed conversion of large recording files to .mat format (RTLABTT-1347)
- RT-LAB/DataLogger: Fixed usage of DataLogger in projects with multiple models (RTLABTT-1339)
- RT-LAB/DataLogger: Recording files are now closed when recording is stopped instead of at model reset (RTLABTT-910)
- RT-LAB/DataLogger: Cleaned configuration parameters (RTLAB-2361)
- RT-LAB: Fixed a problem with the Controller when a model is recompiled after renaming the top-level subsystems (RTLABTT-1342)
- RT-LAB: "Clean project infos" now appears in the right-click menu of a project when it is closed, but still active (RTLABTT-1017 and RTLABTT-972)
- RT-LAB: Fixed compilation of models with parameters of type complex (RTLABTT-1323)
- RT-LAB: Fixed compilation of models with "For Each Subsystem" blocks (RTLABTT-1257)
- RT-LAB: Fixed compilation of models with MATLAB R2015b 64-bit when compiler is set to MinGW64 (RTLABTT-245)
- RT-LAB/Orchestra: Removed duplicated TrimFunction from Orchclickselect.m (RTLABTT-1326)
- RT-LAB/DINAMO: Removed useless pop-ups (RTLAB-2347)
- ePHASORSIM: Bug fix in FMUCReator to install OpenModelica (Ver. 1.9.1) on Linux target (EPTT-80, EPTT-81)

Improved Documentation and Error Reporting

- RT-LAB: New PDF documentation for DataLogger, LabVIEW, and Save/load configuration (RTLABTT-1378)

Version 11.3.3

Features

- ePHASORSIM: New environment variables to do network/data validations and get more logs and verbose output (EP-1382 and EP-1385)

- ePHASORSIM: FMU interface now needs platform individual based FMUs, instead of one file that includes both. All the FMU built in previous versions must be regenerated with FMUCreator in this version (EP-1372)

- MIL-STD-1553: Added support of QPCX-1553 4 channels card (DRV-2701)

- OP4200: Added option to enable/disable automatic bitstream reprogramming (DRV-2777)

- RT-LAB/DINAMO: Added new example model

Bugfixes

- RT-LAB: Fixed application of PARAM_VECTOR_SIZE_LIMIT variable. Very useful for DINAMO (RTLABTT-1216)

- RT-LAB: Fixed projects that were not closing when variable table contains signal and is opened (RTLABTT-1214)

- RT-LAB: Fixed "ConfigModifiedPinger: java null pointer" that may appears sometimes (RTLABTT-1251)

- RT-LAB: Fixed many problems related to variables table refresh (RTLABTT-1241, RTLABTT-2241, RTLABTT-1226)
- RT-LAB: Fixed MATLAB variable support: remove support for vectors and structures (RTLABTT-1220)
- RT-LAB/DINAMO: Fixed many problems and crash when using PEST (RTLABTT-1242, RTLABTT-1243, RTLABTT-1244, RTLABTT-1246, RTLABTT-1247)
- Synchronization: Fixed advanced parameters when synchronized by IRIG-B or 1PPS (DRVTT-555)
- RFM: Fixed release of DMA memory buffer (DRVTT-531)
- OP4200: Fixed remote bitstream programming (IOSFP-264)

Version 11.3.2

Features

- RT-LAB/DataLogger: New "Recorders" section in the project explorer and minor GUI enhancements in order to improve the workflow of the data logging system (RTLAB-2213)
- RT-LAB/DataLogger: Added auto-naming feature for data logging files to prevent conflicts (RTLABTT-1151)
- RT-LAB/DataLogger: Signals are now automatically recorded in data logging files when added to a signal group (RTLABTT-892)
- RT-LAB/DataLogger: Added the possibility to delete obsolete recorders through the contextual menu in the project explorer (RTLABTT-855)
- RT-LAB/DataLogger: By default, hide trigger options in data logging configuration (RTLABTT-1146)
- RT-LAB: Added support for MS Visual Studio 2010 x64 (RTLAB-2178)
- RT-LAB: Upgraded WxBase library from 2.8 to 3.0 in order to reduce some controller crashes (RTLAB-2148)
- RT-LAB: New icons for Edition (default) and OP6000 perspectives (RTLABTT-195)

- Added support of Encoder inputs and Encoder outputs on OP4200 system (DRV-2478)
- Added support of Modbus master on OP4200 system (DRV-1857)
- CAN: Added support for CAN-FD communication (DRV-2263)
- MuSE: Added support of programming new bitstreams on remote OP4510, VC707 and OP4200 systems (IOSFP-202)
- IEC61850: Automatically set synchronization state flag when Oregano card is synchronized using 1PPS or IRIG-B (DRV-2649)
- C37.118 slave: Added an option to round the fraction of seconds to emulate perfect timestamp (DRV-2634)

Bugfixes

- RT-LAB/DataLogger: Fixed cases where data logging trigger was inappropriately activated (RTLABTT-1070)
- RT-LAB/DataLogger: Fixed synchronization issues between signals recorded by data logging system and variable table view (RTLABTT-875, RTLABTT-1041, RTLABTT-1094, RTLABTT-1211)
- RT-LAB/DataLogger: Corrected transfer and conversion to MAT/CSV of data logging files when there are several subsystems (RTLABTT-1044, RTLAB-2179)
- RT-LAB/DataLogger: Made conversion to MAT/CSV of data logging files more robust (RTLABTT-1055)
- RT-LAB/DataLogger: Corrected 'Load configuration' operation for data logging information (RTLABTT-984)
- RT-LAB: Fixed Get parameter function which may not read latest value from the model in some conditions (RTLABTT-757)
- RT-LAB: Fixed OpPlotFile block in order for signal names to be present in file header. This assures compatibility with DINAMO (RTLABTT-1111)
- RT-LAB: Forced 'RTWVerbose' option to 'on' to prevent errors in code generation (RTLABTT-1202)
- RT-LAB: Forced 'GRTInterface' option to 'on' to prevent errors in creation of console subsystem (RTLABTT-1027)

- RT-LAB: Fixed retro-compatibility of connection information in projects made with older versions of RT-LAB (RTLABTT-1167)
- RT-LAB: Fixed 'Cancel' button in 'Load configuration' pop-up (RTLABTT-1143)
- RT-LAB: Spaces are now allowed in the name of project configurations (RTLABTT-625)
- RT-LAB: Fixed issue when opening configuration editor for certain projects (RTLABTT-762)
- RT-LAB: Fixed 'Rename' operation for I/O interfaces (RTLABTT-1205)
- ePHASORSIM: Fix pins for three-phase voltage source (EPTT-63)
- ePHASORSIM: Bus validation logic and error logs (EPTT-68)
- Modbus master: Fixed segmentation fault occurring in RTU mode when no slave is connected (DRV-2629)
- IEC61850: Fixed ICD parser for multiple IEDs per file (DRV-2672)
- DNP3 slave: Fixed the retrieval of the analog/binary event modes (DRVTT-491)

Improved Documentation and Error Reporting

- RT-LAB/DataLogger: Added new example project that explains how to use data logging system (RTLABTT-916)
- RT-LAB: Added verification on 'separate.exe' before model separation and explicit error message (RTLABTT-1138)

Version 11.3.1

Features

- Added support for Modbus master driver

Bugfixes

- Fixed crash when using DINAMO Parameter estimation (RTLABTT-942)

Version 11.3.0

Features

- RT-LAB/DataLogger: New data logging system with continuous and triggered recording capabilities (RTLAB-1536)
- RT-LAB/DataLogger: New acquisition source in ScopeView for new data logging system (RTLAB-1536)
- RT-LAB/DataLogger: New "data" folder in project explorer in order to easily access recorded simulation data (RTLABTT-870)
- RT-LAB: New "scripts" folder in project explorer for editing and executing Python scripts (RTLABTT-650)
- RT-LAB: Support of Simulink SLX file format (RTLAB-1959)
- RT-LAB: Support of Simulink dashboard blocks for prettier console subsystems (RTLAB-1959)
- RT-LAB: New RT-LAB logo! (RTLAB-1959)
- RT-LAB: New license file is needed for OS verification (RTLAB-2134)
- RT-LAB: At load of model, the active view is "Display" instead of "Variable Table" (RTLABTT-385)
- ARINC-429: Added new dynamic driver interface for Abaco PCIe card (DRV-2044)
- DNP3 slave: Added support of the new configuration interface (DRV-2335)
- DNP3 master: Added support of the new configuration interface (DRV-2336)

- MuSE: Added support of OP5707 and OP4510 as central systems (IOSFP-270)
- MuSE: Added MAC address management for remotes OP4200 (IOSFP-215)
- ePHASORSIM: Single cage and double cage induction generator (EP-1164)
- ePHASORSIM: Adjustable (internal voltage and impedance) 3-phase voltage source (EP-1250)
- ePHASORSIM: New version for Excel template (V1.6) and new components (EP-1087)
- ePHASORSIM: Multiphase transformer for distribution systems (EP-1173)
- ePHASORSIM: A new example (PHASOR-22) with induction generators (EP-1165)
- ePHASORSIM: Detailed report about partitioning if number of partitions is greater than 1 (EP-1167)

Bugfixes

- RT-LAB: Better performance when setting parameter values with API functions (RTLAB-2055)
- RT-LAB: Better performance when creating aliases on OpInput and OpOutput blocs (RTLABTT-880)
- RT-LAB: OpenProject API function works in multi-thread or multi-process context (RTLABTT-681)
- RT-LAB: Negative time factors in Load and Execute API functions are forbidden (RTLABTT-619)
- RT-LAB: Setting embedded mode no longer returns "Unable to create embedded simulation" error (RTLABTT-606)
- RT-LAB: Embedded mode works with models without SC subsystem (RTLABTT-792)
- RT-LAB: Fixed several issues when saving or loading project configurations (RTLABTT-751, RTLABTT-940, RTLABTT-755, RTLABTT-876, RTLABTT-723)
- RT-LAB: Restoration of active project configuration is now possible in case of crash (RTLABTT-814)

- RT-LAB: Fixed Controller crash when it is unable to communicate with a model (RTLABTT-776)
- OPAL-RT Boards: Renamed the board types in the drop down list to have a more intuitive meaning (DRV-2539)
- ePHASORSIM: Including the impact of multiphase shunt status in power-flow (EPTT-51)
- ePHASORSIM: Fix in CYME converter for susceptance units (uS as opposed to S) for Overhead Balanced Lines when converting to a multiphase network (EPTT-45)

Improved Documentation and Error Reporting

- RT-LAB: Added documentation for OpenProject and CloseProject API functions (RTLABTT-222)
- RT-LAB: Updated obsolete "Model not specified by previous OpalConnect or OpalSetCurrentModel" error message (RTLABTT-340)

Deprecation and Removals

- RT-LAB: Removed obsolete third-party I/O blocs (Acromag IP, Brandywine PCI SyncClock32, Concurrent FBSSync, NI PXI/PCI-7831, Quanser Q8, SBS Technologies IP) (RTLAB-2128)
- RT-LAB: Support of MATLAB R2011b is deprecated. It will be abandoned in RT-LAB 11.4 (RTLABTT-772)
- RT-LAB: Support of Python 2.2, Python 2.3, Python 2.4, and Python 2.5 is deprecated. It will be abandoned in RT-LAB 11.4 (RTLABTT-781)
- RT-LAB: SetCurrentModel, ConnectByName, and Disconnect API functions are deprecated (RTLABTT-221)
- ePHASORSIM: In Excel V1.6 these components are obsolete and must be replaced by their corresponding multiphase pairs: Line 3-phase, Load 3-phase, Shunt 3-phase, Bus Faults 3-phase

Version 11.2.3

Features

- RT-LAB: Improved the delay when creating a connection to LabVIEW panels when the model is running (RTLABTT-557)
- ePHASORSIM: Import three-winding transformer from PowerFactory
- ePHASORSIM: Added new example with a 2000 bus synthetic network (PHASOR-20)

Bugfixes

- RT-LAB: Fixed quality issues with the Controller that manages the targets (RTLABTT-636)
- RT-LAB: Fixed quality issues with the embedded mode (RTLABTT-598, RTLABTT-606)
- RT-LAB: Fixed project configuration pop-up when parameter values change (RTLABTT-621)
- RT-LAB: Fixed conflict between the LoadParameters function and the Variable Table (RTLABTT-640)
- RT-LAB: Fixed a compilation issue with Stateflow models (RTLABTT-660)
- RT-LAB: Fixed a registry key conflict between MATLAB R2011a and R2011b (RTLABTT-653)
- RT-LAB: Fixed dependency of launch sequence on LabVIEW run-time engines (RTLABTT-590)
- RT-LAB: Fixed hanging of the RT-LAB.exe process at close of program (RTLABTT-544)
- RT-LAB: Fixed the appearance of the "Build configurations" window when there is no development node. (RTLABTT-160)
- ePHASORSIM: Fixed for *.DZ file in PHASOR-17 example

- ePHASORSIM: Revisions for *.DGS and *.PDF files in PHASOR-17 and 19
- ePHASORSIM: Corrections for project paths for RT-LAB import

Version 11.2.2

Features

- RT-LAB: Added support for MATLAB R2017a
- RT-LAB: Added possibility of editing parameters when the model is not loaded. Parameter values can be saved in project configuration (RTLAB-1880)
- RT-LAB: Added support of new bitstream names (RTLABTT-470, RTLABTT-485)
- RT-LAB: Added OS license (RTLAB-1890)
- RT-LAB: Added a "Show in project explorer" option from a LabVIEW panel (RTLABTT-498)
- RT-LAB: Added Lock project mode (RTLAB-1882)
- RT-LAB: Added version number to libraries and executables (RTLABTT-372)
- RT-LAB: Added file mode in signal generator I/O (RTLAB-1885)
- RT-LAB: Added a single scope panel in the "New RT-LAB Panel" wizard (RTLABTT-456)
- RT-LAB: Added Visual Studio Code as a debugging tool (RTLAB-1903)
- RT-LAB: Added data logger synchronous mode (RTLAB-1920)
- RT-LAB: Added data logger automatic file transfer (RTLAB-1809)
- RT-LAB: Added possibility of converting data logger file (.oprec) to .csv or .mat (RTLAB-1929)
- RT-LAB: Improved Simulink error management (RTLABTT-268)
- RT-LAB: Improved RT-LAB installer in order to have a single file (RTLAB-1894)
- RT-LAB: Improved default columns in Variable Table (RTLAB-1918)

- C37.118 master: Added support of the new configuration interface (DRV-2108)
- IEC 60870-5-104 slave: Added support of the new configuration interface (DRV-2210)
- IEC 60870-5-104 slave: Added support of RMS calculation for floating point outputs (DRV-2094)
- OP4200: Added support of 1GHz CPU (DRV-2151)
- OP4200: Added support TSD inputs and TSD outputs (DRV-2230)
- Profibus: Added support of master and slave interfaces (DRV-2190)
- OP5368: Added support of card (DRV-2251)
- I/O SFP: Added partial support for remote I/Os controlled by SFP (DRV-2224)
- ePHASORSIM: Added import from PowerFactory DGS file supports FMU
- ePHASORSIM: Added import from CYME is extended to support multiphase transformer, synchronous generator, PV
- ePHASORSIM: Added new example for Microgrid with PV integration as FMU(PHASOR-18)
- ePHASORSIM: Added new example for PowerFactory input files with FMU (PHASOR-19)
- ePHASORSIM: Added new FMU based components are added, check the user guide to see the complete available items
- ePHASORSIM: Improved impedance of Pi-Line in positive sequence can be tuned during simulation
- ePHASORSIM: Improved bug fix for FMUCreator on Windows 10

Bugfixes

- RT-LAB: Fixed restoration of connections and aliases when a bus structure is modified (RTLABTT-425)
- RT-LAB: Fixed some API functions that do not return errors (RTLABTT-428)

- RT-LAB: Fixed wrong detection of LabVIEW run-time engines on a 32-bit Windows PC (RTLABTT-494)

Deprecation and Removals

- RT-LAB: Removed the possibility of saving the project configuration when the model is loaded

- RT-LAB: Removed OpalNode and transferred its functionality to MetaController and OpTargetD (RTLAB-1895)

- RT-LAB: Removed MATLAB embedded view from RT-LAB (RTLABTT-433)

Version 11.2.1

Features

- RT-LAB: Added support for MATLAB R2015b to MATLAB R2016b and partial support for MATLAB R2017a. *Note that Artemis, RT-Events and eFPGAsim are not compatible with MATLAB R2017a

- RT-LAB: Added support of mixed SignalGroup with and without trigger in Datalogger (RTLAB-1755)

- RT-LAB: Added option to edit the default number of samples per signal in ProbeControl

- RT-LAB: Improved configuration workflow (RTLAB-1870)

- RT-LAB: Improved OP6000 mode launch and I/O cards icons (RTLAB-1780 RTLAB-1883)

- RT-LAB: Improved RT-LAB blocks documentation (RTLABTT-2 RTLABTT-371)

- CAN: Added support for multiple Kvaser cards in the same system (DRV-2109)

- C37.118 master: Added option to run the driver on a dedicated core (DRV-2105)

- IEC 61850: Added support to run the driver on Windows (DRV-2128)

- IEC 61850: Added option to control the simulation flag and to retrieve both simulation flag and test bit (DRV-2129)
- IEC 61850: Added option to enable all Sampled Values and GOOSE transmission/reception by default at the beginning of the simulation (DRV-2129)
- IEC 61850: Added support for fixed-length encoding of GOOSE messages as per IEC 61850-8-1 Ed.2 A.3 (DRV-2129)
- EtherCAT master: Added support of EL3161 module

Bugfixes

- RT-LAB: Fixed eHS automatic connections with OP4200 (RTLABTT-355)
- RT-LAB: Fixed loss of connections and options after renaming a LabVIEW panel (RTLABTT-423 RTLABTT-424)
- RT-LAB: Fixed offline use of OpInput block (RTLABTT-422)
- RT-LAB: Fixed project explorer not showing OpInput and OpOutput folders (RTLABTT-352)
- RT-LAB: Fixed shortcuts removal after uninstalling RT-LAB (RTLABTT-468)
- RT-LAB: Fixed issue with GUI button when switching to embedded mode (RTLAB-1437)
- RT-LAB: Fixed RT-LAB DINAMO license checking (RTLAB-1878)
- RT-LAB: Fixed issue with 2 Matlab process during compilation (RTLABTT-225)
- OP4200: Fixed driver initialization order to allow CAN driver to run with Opalboards driver
- OP4510: Replaced example model bitstream to include a fix on TSD inputs (DRVTT-133)
- C37.118 slave: Fixed issue with 50Hz nominal frequency (DRVTT-206)
- C37.118 slave: Fixed binding with a specific network interface (DRV-2154)
- C37.118 slave: Fixed use of loopback and wlan network interfaces (DRV-2158)

- C37.118 master: Fixed timeout when stopping the simulation (DRV-2172)

Version 11.2.0

Features

- RT-LAB: Added aliases in RT-LAB
- RT-LAB: Added aliases, panels and scripts to rtdemo examples (RTLAB-1833)
- RT-LAB: Added new system to protect connections and alias from loss when moving or renaming block in model
- RT-LAB: Added Import / export workspace (RTLAB-1773)
- RT-LAB: Added new templates in panels section (RTLAB-1853)
- RT-LAB: Added variable table visible when execute model (RTLAB-1819)
- RT-LAB: Added possibility to run TD2.8 scripts (RTLAB-1765)
- RT-LAB: Added the creation of connections in the API (RTLAB-1812)
- RT-LAB: Added error messages when a connexion is refused (RTLAB-1812)
- RT-LAB: Added possibility to display captions or labels in LabVIEW panels (RTLABTT-336)
- RT-LAB: Added LabView panels accessible by default
- RT-LAB: Added new TestDrive projects
- RT-LAB: Added Save / Load configuration
- RT-LAB: Added possibility to delete a configuration (RTLAB-1855)
- RT-LAB: Added Save / Load parameters from GUI
- RT-LAB: Added TestDrive perspective
- RT-LAB: Added DataLogger to RT-LAB

- RT-LAB: Added Driver cores protection from being reserved multiple times in multi-subsystem models
- RT-LAB: Improved configuration handling for OP6000 projects (RTLAB-1816)
- RT-LAB: Improved RT-LAB clean option at startup (RTLABTT-177)
- RT-LAB: Improved RT-LAB uninstaller (RTLAB-1812)
- RT-LAB: Updated EULA licence Intel
- RT-LAB: Updated variable table and API to update with LabView widgets
- CAN: Added new solution with support of CANdb parsing, bit-aligned signals and display of message content
- CAN: Added cyclical messages support to Kvaser and OP4200 drivers
- TestDrive: Add support of new hardware based on Linux, OP5142 cards and PCIe communication
- RFM: Add support of GE 5565-PIORC 256M
- IEC61850: Improved timing precision when transmission is synchronized by Oregono card
- Pickering: Added support of 50-295-021-5/12 resistive card
- C37.118 slave: Initialize timestamp to system time when using local synchronization source
- C37.118 slave: Added support of simulation mode on Windows system
- Synchronization: Added support of new profiles on PTP mode
- OP4200: Added support of OPC-UA server interface
- ePHASORSIM: Import from PowerFactory DGS file is added (built-in balanced system)
- ePHASORSIM: Import from CYME is extended for balanced system (built-in and FMU components)
- ePHASORSIM: Import from CYME is extended to support ECG, distributed loads, and voltage regulator, recloser
- ePHASORSIM: Import from PSS/e is extended to include HVDC (as FMU)
- ePHASORSIM: Power-flow supports multiphase components

- ePHASORSIM: Power-flow has Flat Start and Smart Start for initial guesses
- ePHASORSIM: Import from CYME can now use the internal power-flow option instead of CYME's power-flow Excel file
- ePHASORSIM: New demos are added for test automation, modified WECC system, PowerFactory and CYME input files
- ePHASORSIM: Set number of cores to 1 on linux machine if EPHASOR_THREADS is not defined
- ePHASORSIM: PQ measurement outgoing pins are added to multiphase lines
- ePHASORSIM: License update is required to Version 2017.5
- ePHASORSIM: Check Migration Notes in the user guide for mandatory changes

Bugfixes

- RT-LAB: Fixed get value of vector elements always return value of first element (RTLABTT-348)
- RT-LAB: Fixed API function GetActiveModels (RTLABTT-361)
- RT-LAB: Fixed support of 3x3 matrixes (RTLABTT-270)
- RT-LAB: Fixed support of multiple connexions to the same controller (RTLABTT-188)
- RT-LAB: Fixed 1st RT-LAB opening problem with Windows 10 (RTLABTT-213)
- RT-LAB: Fixed compilation for models with fixed-point type (RTLABTT-171)
- RT-LAB: Fixed asynchronous process with gcc (RTLABTT-140)
- Orchestra: Fix stability issues
- IEC61850: Fix order of data attributes in GOOSE message
- ePHASORSIM: Bug fixes for constant current load

Deprecation and Removals

- RT-LAB: Removed Infiniband link (RTLABTT-144)

ARTEMIS

Version 7.6.1

Features

- Compatibility with RT-LAB 2020.2
- New Support of OPAL-RT Linux 3.
- Added Warning and Error message when SPS generate unconnected state-space model preventing a successful compilation of the model.
- Fix Matlab crash when ARTEMiS model is too big.

Version 7.6.0

Features

- Compatibility with RT-LAB 2020.1
- Support Matlab R2019a, R2019b
- New SSN Dual-Stator Synchronous machine model with electric ship demo (sometimes called 6-phase synchronous machine)
- New SSN Dual-Stator Permanent Magnet Synchronous machine model with electric ship demo (sometimes called 6-phase PMSM)
- New SSN Synchronous machine model with Per-Unit mask.
- New SSN Induction machine model with Embedded Breakers.
- New ARTEMiS Event Timer block. Useful to program on/off sequence of switches

Bugfixes

- Improvement to the SSN synchronous machine models: With 'Delayed Speed Term' (DST) option ON, the models are now more stable. With this improvement, the IEEE 39 bus 10 machine demo is now stable with DST enabled. High speed models such as aircraft with 800 Hz stator frequency are now stable with DST ON. DST option allows the use of LDLt factorisation for faster simulations.
- Improvement of OpElectricFaultSelector block icon display.
- Warning is correctly displayed to enforce a non-null thyristor offset voltage when using the ITVC switching compensation algorithm of ARTEMiS.

Version 7.5.0

Features

- Compatibility with RT-LAB 2019.3
- New Standard Per-Unit Synchronous machine model with Canay inductance option
- New demo of Synchronous machine with thyristor inverter and neutral switching assistance
- New ARTEMiS GUIde interface with simplified menu and matrix conditioning test option
- New Moving Train demo with continuously variable rail impedance
- Support of MATLAB versions 2015b and above up to 2018b
- Support of 64-bit OS on target for faster real-time simulation

Version 7.4.1

Features

- Compatibility with RT-LAB 2019.2
- New capability from RT-LAB platform to import ARTEMiS real-time models
- Full iterative feature available in SSN to increase accuracy when simulating power electronic circuits in offline and real-time mode
- New model of transmission line with variable fault location made in SSN. This model improves the previous model with exact loss repartition
- New model of unbalanced 3-phase pi-line (not available in Simscape Electrical formerly SimPowerSystems)
- New model comparing Wideband and FD-line model for 300km untransposed 735kV line using the new OPAL-RT line fitter
- New model (UCB_8ports) for 8-port SSN-UCB
- New beta model to define an SSN group with a SPICE netlist (ssn_supra_smallHVDC.slx)

Bugfixes

- Fix to the SPS LineParameter.p file that was producing wrong line data for the new WB and FD-line fitter

Improved Documentation and Error Reporting

- New application note on how to obtain SI parameters from PU-standard for the SSN Synchronous machine model

Version 7.4.0

Features

- Compatibility with RT-LAB 2019.1
- Support Matlab R2018a, R2018B
- New SSN Wideband model (2-4-6 phase available) with simple fitter data input; the model has been validated with Hypersim
- New Marti FD-line model (3 phase only, beta) with simple fitter input.
- New SSN Wideband fitter GUI for lines and cables. Cable option is new and is made from Hydro-Quebec Crinoline routines. The Fitter GUI produces a (.dat) fitting file directly usable by the new Wideband model of SSN.
- New demo and new beta block of 3-phase Distributed Parameter Line with variable fault position. This demo is made with SSN methodology: losses are now exactly splitted on both sides of the fault (as opposed to the similar non-SSN model which assumes a 50/50 repartition for all fault positions) R2015a+ only

Bugfixes

- Fix of Active Distribution Grid with High Penetration of Distributed Generation using SSN
- Fix of SSN Dynamic load demo: now using low pass filter in RL calculation for improved stability
- Fix of SSN Synchronous machine models (with and without neutral terminal), 6th order
- Fix of SSN Parallel RLC and SSN Series RLC blocks: corrected delay on B matrix, similarly done in SSN machines in earlier fixes
- Fix of OLTC SSN model in artemis.mdl for proper automatic S-function building
- Fix of Simple inductance SSN demo

Improved Documentation and Error Reporting

- Added demo: MMC HVDC link using TSB-type model (model coming directly from the MMC blockset)

- Added demo: MMC HVDC link using SSN User-Custom-Model in one station; gives better accuracy than TSB-type in rectifying modes
- Added documentation about line/cable model selection and fitters.

Version 7.3.6

Features

- Compatibility with RT-LAB 11.3.6

Version 7.3.4

Features

- Compatibility with RT-LAB 11.3.4
- Added support of MatLab R2017b
- TLC file available for 2-level TSB-RD for faster real-time simulation

Bugfixes

- Bug corrected in tsb2level_RD and tsbT_RD

Improved Documentation and Error Reporting

- New multi-rate demo using multi-rate DPL in 48-pulse STATCOM application

- New 20 kHz T-type inverter demo in solar power application
- New Kundur 4 machine demo in RT-LAB format
- Updated SSN machine paper and PPT

Version 7.3.2

Features

- Compatibility with RT-LAB 11.3.2
- New TSB model (TSB-RD) 2-level
- New TSB model (TSB-RD) 3-level NPC (2 and 3 phases)
- New TSB model (TSB-RD) 3-level T-type (RD stands for real diodes)
- Note: previous TSB models are still available
- Improved switch matrix permutation calculation speed in offline mode and in RT-LAB model separation.

Improved Documentation and Error Reporting

- New TSB-RD demo section in ARTEMiS on-line demos
- New application note: How to decouple a model
- New application note: Switch models in ARTEMiS
- New application note: How to adjust RC snubber for TSB
- New application note: About Park Transforms
- New application note: LU vs LDLt factorizations in SSN

- New Application Note section in ARTEMiS Demos (under Scientific paper and benchmark section)
- Online Demos reorganized to be unique across matlab versions and placed in the common folder of the installation
- Added some papers and PPT in ARTEMiS scientific paper section.

Version 7.3.0

Features

- Compatibility with RT-LAB 11.3.0 and with RT-LAB 11.3.1
- SSN synchronous machine block with backward Euler option

Bugfixes

- SSN OLTC blocks: small correction in no saturation mode made to allow compilation to complete
- 3-level NPC demo: correction to allow DC bus to charge correctly considering null initial conditions

Improved Documentation and Error Reporting

- New paper on SSN rotating machine included in examples section
- New application notes section in examples section

Version 7.2.3

Features

- Compatibility with RT-LAB 11.2.3
- Renamed "SSN Ground Referencing Resistor" block.

Bugfixes

- Fixed certain RT-LAB compatible online demos: `ssn_9LevelDrive_xfozigzag`, `ssn_DFIM_wind_turbine_with_crowbar` and `SSN_IEEE_123Node`.
- Correction to SSN resistance model.

Improved Documentation and Error Reporting

- Added documentation for Artemis decoupling blocks and editable sample time.

Version 7.2.2

Features

- Compatibility with RT-LAB 11.2.2
- Compatibility MATLAB 2011b, 2015a-SP1 (preferred version), R2016b, R2017a (64 bits)
- SSN solver and discretization methods are now used for all electric subsystems, even if the model is not modeled with SSN (flag `DISABLE_SSN_FOR_NON_SSN_MODELS` can be used to use old state-space S-function)

- SSN initial conditions now set to 0 automatically
- New Kundur 4-machine, 2-area model with SSN synchronous machine
- SSN printout of matrix inversability condition number when USE_MFILE_SSN_SFUNCTION=1 is set in workspace
- Updated 3 winding 3-phase OLTC transformer demo using SSN: now without S-function builder block.
- 3-level NPC TSB model: ground connections are now implicit.

Bugfixes

- Code correction in SSN-OLTC model v2 (without S-function)

Improved Documentation and Error Reporting

- Added scientific paper section to the demos
- Added benchmark section to the demos
- New IEEE 123 node test feeder using SSN demo
- Bipolar HVDC with switched filter banks online demos modified to have better numerical response with LDLT solver.
- New SSN demo containing distributed parameter line with breakers and faults at both ends

Version 7.2.1

Features

- Compatibility with RT-LAB 11.2.1
- RT-LAB snapshot functionality for Simscape Power Systems `sfun_discreteVariableDelay` S-Function. This allows support for the following blocks: in `powerlib_meascontrol/Measurements`: Fundamental(PLL-Driven), Mean(Variable Frequency), Positive-Sequence(PLL-Driven), Power (PLL-Driven, Positive-Sequence); and also in `powerlib_meascontrol/PLL` blocks.

Improved Documentation and Error Reporting

- Major scientific papers at ARTEMiS-SSN now accessible in the on-line demo section
- SSN benchmarks accessible in the on-line demo section
- Various small corrections to demo models

Version 7.2.0

Features

- Compatibility with RT-LAB 11.2
- Compatibility MATLAB 2011b, 2015a-SP1 and R2016b (preferred versions)
- New LDLT Factorization option in SSN to improve real-time speed.
- Adding Delayed Speed Term option in most SSN rotating machine models (SM, DFIM and PMSM)
- Model updates for SSN-SM: more measurements available
- New SSN Custom models available: Parallel RLC, Series RLC, R, all with on-line changeable RLC parameters.
- Quadruple precision precalculation in SSN using `op_ssn_online_quad_precision_inversion` workspace variable. This flag makes ARTEMiS precalculation routine uses quadruple precision floating point arithmetic for all matrix inversions, on the target only. Windows and Microsoft Visual Studio donâ€™t

support quadruple precision, therefore the option will only have an effect during real-time simulation on Linux targets.

- New Reconfigurable breaker model available with script and demo. Using this model, one can turn breakers into fixed/closed circuits using a single model running multiple test scenarios.

- Removal of iteration printouts by default in offline mode. `op_ssn_print_iteration_info` variable must be set in workspace now.

Bugfixes

- Major bug correction for SSN solver affecting Rotating machine models mainly: the model admittance matrix was copied in the global system admittance matrix in a transposed way. The copy of the admittance matrix is now correctly done. This only affect machine models, without delayed speed terms, because these have asymmetric matrices.

- Model corrections to SSN-SM and SSN-DFIM to have a delayed discrete B matrice used during SSN model calculation. This delayed B matrice corrects a discrepancy between internally computed current and external ones in case with machine connected to very small loads.

- Installer correction: IEEE 39 bus 10 machine demo is now really accessible

Improved Documentation and Error Reporting

- HELP available for iMOV, TSB 2-level, TSB 3-level and other blocks

- SSN Dynamic load demo available. More stable than injection-based dynamic load of SPS. (beta version)

- New RT-LAB and ARTEMiS SSN Monte-Carlo test demo using snapshot feature

RT-EVENTS

Version 4.6.1

Features

- Added support of OPAL-RT Linux 3
- Provided compatibility with RT-LAB 2020.2

Bugfixes

- Fixed crash when starting simulation while driving a RTE block with a Simulink Ground

Version 4.6.0

Features

- Added support for MATLAB versions R2019a and R2019b
- Provided compatibility with RT-LAB 2020.1

Version 4.5.0

Features

- Provided compatibility with RT-LAB 2019.3

Version 4.4.1

Features

- Provided compatibility with RT-LAB 2019.2

Bugfixes

- Fixed a bug where the RTE signal would not be initialized in the right order when using atomic subsystem for recent matlab versions (V >= 2016a)

Version 4.4.0

Features

- Added support for MATLAB versions R2018a and R2018b
- Provided compatibility with 2019.1

Version 4.3.4

Features

- Added support for MATLAB versions R2017b
- Provided compatibility with RT-LAB 11.3.4.

Version 4.3.2

Features

- Provided compatibility with RT-LAB 11.3.2 and RT-LAB 11.3.3.

Version 4.3.0

Features

- Provided compatibility with RT-LAB 11.3.0 and RT-LAB 11.3.1.
- RT-LAB snapshot supported for all RT-EVENTS blocks

Version 4.2.3

Features

- Provided compatibility with RT-LAB 11.2.3.

Version 4.2.2

Features

- Provided compatibility with RT-LAB 11.2.2.

Version 4.2.1

Features

- Provided compatibility with RT-LAB 11.2.1.

Version 4.2.0

Features

- Provided compatibility with RT-LAB 11.2.0.
- Added support for MATLAB versions R2015b, R2016a, R2016b and R2017a, including support for 64 bit versions.(EMSTT-53)

Bugfixes

- Fixed bug where rte_scope crashes during offline 64 bit Simulink simulation.(EMSTT-52)
- Fixed bug in rte_filter where rise time and fall time occur in consecutive calculation steps, and time between them is shorter than the filter pulse width. Rise was incorrectly moved to start of its calculation step. Now rise time is correctly moved to start of the next calculation step which also contains fall time.(EMSTT-48)
- Fixed bug introduced in version 4.1.4 that caused offline simulink simulations that contained rte signals to crash.

Version 4.1.4

Features

- Provided compatibility with RT-LAB 11.1.4.

Version 4.1.3

Features

- Updated encoder and event detector demos so that they function with Matlab R2015aSP1

Improved Documentation and Error Reporting

- Added Matlab help landing page for RT-EVENTS

Version 4.1.0

Features

- Provided compatibility with the RT-LAB 11.1 product family.
- Added non-blocking warnings to suggest upgrading old TSB models to new ones with high-impedance and rectification support. This warning can be disabled by defining variables (ex: DISABLE_NEW_2LEVEL_TSB_NOTIFICATION) in the workspace.

Version 4.0.2

Features

- Added support for Matlab R2015a (Service Pack 1).

Version 4.0.1

Features

- Added support for Matlab R2014b.

Version 4.0.0

Features

- Provided compatibility with the RT-LAB 11.0 product family. (TT#8492)

Version 3.9.0

Features

- Added support for Matlab versions R2012a, R2012b and R2013a. (TT#7891)

Version 3.8.0

Features

- Modify documentation format to allow compatibility with RT-LAB documentation. (TT#6820)

Bugfixes

- Fixed 2 level tsb high z block cannot be compiled with RT-LAB. (TT#7022)

Version 3.7.0

Features

- Added support for MatLab R2011b. (TT#6952)

Version 3.6.0

Features

- Added support for Matlab R2011a. (TT#6662)

Version 3.5.0

Features

- Added support for Matlab R2010a and R2010b. (TT#6393)

eFPGA_{sim}

Version 2.3.3

Features

- Added support for BLDC Motor model with the Schematic Editor (EFS-2435)
- Added autoconfiguration of the eHS block from conf file (EFS-2437)
- Added BackEmf outputs support on PMSM and BLDC Schematic Editor block (EFS-3256)
- Added Hall effect support PMSM and BLDC Schematic Editor block (EFS-3257)
- Support of FPGA scope in OP4510 IOConfig1 firmwares (EFS-3336)
- Added support of PMSM DQ and BLDC in the Generic machine block (EFS-2982)
- Added RCP firmware with eHS for OP4200 (EFSTT-834)
- Added DQ-transform angle offset support for the PMSM VDQ in the Schematic Editor. VDQ parameters file update required (EFS-3473)

Bugfixes

- Separated PMSM's Encoder speed ratio and theta offset from resolver's (EFS-3309)
- Fixed an issue with Generic machine callback that did not initialize wCarFreqRes (EFSTT-848)
- Fixed an issue with log files and DO reports of eHS being locked (EFS-3151)
- Fixed issue making the eHS (Schematic Editor workflow) load circuit crash when adding an input to models which previously had none (EFSTT-839)
- Added a port dimension assertion of 1 (one) to the eHS block (Schematic Editor workflow) input ports (EFSTT-717)

Version 2.2.1

Features

- Added support for PMSM SH in Schematic Editor (PMSM SH needs 1,536 MB of MATLAB Java Heap Memory to work in Schematic Editor) (EFS-2438)
- Added support of Matlab R2019A and R2019B (EFS-2909)
- Added tool for converting motor model files (RTT, ANSYS) into Schematic Editor compatible formats
- Added support of Gs and Turn ratio tuning in transformer (EFSTT-720)
- Added new firmware for eHSx32 support on OP4200 (EFS-3084)
- Added support of selecting xls sheet for scenarios in eHS CPU block (EFS-3080)

Bugfixes

- Fixed issue with user analog output assignement with AOMR V2 (EFSTT-780)
- Fixed issue with AOMR V2 having offset in user analog out signals (EFSTT-770)
- Fixed issue with AOMR V2 Console block not saving properly its values (EFSTT-769)
- Fixed issue with the generic machine block that does not update its imports and outputs while using 2 machines or more (EFSTT-790)
- Fixed crash in Matlab R2016b while using two machine interface blocks (EFSTT-796)

Deprecation and Removals

- Removed support of Matlab R2014B

Version 2.1.2

Features

- Added support of SCIM in Schematic Editor workflow
- Added example Model SCIM OP4510 and OP5700
- Added support of DFIM in Schematic Editor workflow
- Added example Model DFIM OP4510 and OP5700
- Added support of PMSM Variable DQ in Schematic Editor workflow
- Added example Model PMSM Constant DQ OP4200, OP4510 and OP5700
- Added example Model PMSM Variable DQ OP4200, OP4510 and OP5700
- Added support of Synchronous Machines with neutral point in SPS workflow
- Added eHSx16 form factor
- Added AOMR v2 CPU block for SPS workflow

Bugfixes

- Fixed issues with installation process of eFPGASIM causing exceptions and crashes during normal utilization (EFSTT-640)
- Fixed issue when using eHS gen 4 block when Ts was not declared (EFSTT-625)
- Fixed issue with Digital Out not working with the OP4200 firmware with machines on Schematic Editor (EFSTT-586)
- Fixed issue with excitation input for resolvers only mappable to analog in channel 1 on Schematic Editor (EFS-2693)
- Fixed bitstream mismatch warning for VC_707 eHSx128 (EFSTT-648)
- Fixed organize examples in SPS and SE sub folders (EFSTT-643)

- Fixed error when clicking Edit then Cancel on eHS SPS block (EFSTT-605)
- Fixed source naming in configuration window (EFSTT-580)
- Fixed circuit file name not updating correctly when modified (EFSTT-579)
- Improved the error message while two current measurements are touching in SPS netlist (EFSTT-577)

Version 2.0.0

Features

- Added support of PMSM on OP4200 in Schematic Editor workflow
- Added support of Saturable Transformers in SPS workflow
- Added support of new circuit editor : OPAL-RT Schematic Editor
- Added support of frequency dependent lines to eHS, with demo example. (EFS-2182)
- Added support of eHS Gen4 core in the XSG library. Gen3 and earlier versions of eHS are deprecated (EFS-2289)
- Added AOMR v2 that is capable of routing and rescaling from eight FLWS signals to analog out channels. (OPAL1-523)
- Analog In Re-scaling (AIR) block now supports Min and Max parameters and saturates output accordingly. (EFS-2168)

Version 1.5.7

Bugfixes

- Fixed support for MATLAB R2018b (EFSTT-517)

Version 1.5.6

Features

- Added official support of MATLAB version 2017b

Version 1.5.5

Features

- Added official support of MATLAB versions 2018a and R2018b
- Added support of the thermal losses for eHSx64 (EFSTT-459)

Bugfixes

- Fixed DC offset issue with 3 level LCA (EFSTT-396)
- Fixed issue while parsing the name of a LCA bridge ends with trailing spaces (EFSTT-367)

Version 1.5.4

Features

- Added standard motor package for OP5700 (EFS-1667)
- Added demos for eHS with PMSM with and without I/Os for OP5700 (EFS-1870)

- Added demos for eHS with DFIM with and without I/Os for OP4510 and OP5700 (EFS-1890, EFS-1886)
- Added demos for eHS with SCIM with and without I/Os for OP4510 and OP5700 (EFS-1889, EFS-1887)
- Added demos for eHS with SRM with and without I/Os for OP4510 and OP5700 (EFS-1891, EFS-1888)
- Added demo for a eHS with PMSM SH and IOs for OP4510 (EFS-1919)
- Added standard motor package for OP4510 with Kintex-7 410t (EFSTT-265)
- Added time-stamped T-Type converter feature to use with eHS (EFS-1987)
- Added two inputs dot product feature to use with eHS (EFS-1987)

Bugfixes

- Fixed netlist creation issues when using both Lca and non-Lca switches in same circuit model (EFSTT-237, EFSTT-269)
- Fixed a bug preventing from using multiple inverter solver blocks with different parameter sets (EFSTT-202)
- Fixed Sine Wave Generator output mapping issue (EFSTT-158)

Version 1.5.3

Features

- Added official support of Matlab versions 2015b, 2016a, 2016b and R2017a
- Performance improvement of eHS during update and build of the CPU model (EFS-1177)
- Added standard motor package for OP4510 (EFS-1671)

- Added official support for OP4200 1GHz (EFS-1843)
- Added demo for a eHS with PMSM and IOs for OP4510 (EFS-1687)
- Added OP4510 eHS with machine firmware (EFS-1685)
- Added support for eHSx128 in eFPGASIM XSG library (EFSTT-85)
- Added XFO support in PLECS (EFS-463)
- It is now possible to change the Flux value of the PMSM VDQ block on the fly (EFS-1797)
- Added support of eHS circuits without state (EFSTT-4)
- Added support of *.xlsx file format to the eHS Scenario feature (EFSTT-40)
- Removed the eHS Gen2 CommBlk from library (EFSTT-178)
- Removed MMC Example models from available demos

Bugfixes

- Fixed AOMR Jitter issue (EFSTT-18)
- Fixed typo in eHSx32 for OP4200 mask (EFSTT-131)
- Fixed mixed up results for Thermal Losses when increasing the number of converters (EFSTT-160)
- Fixed issue when changing the number of external inputs of eHSx128 (EFSTT-163)

Version 1.5.2

Features

- Added Beta support of Matlab versions 2015b, 2016a and 2016b. (EFS-1457)

- Added the loss calculation module for 2-level bridges of eHS (EFS-1109)
- Added the option of "eHSx128 + custom field" in the AOMR console block (EFS-1465)
- Added support of firmware generation with eHSx128 (EFS-1175)
- Added a monitoring feature to evaluate the local min and max of eHS outputs for a CPU time step (EFS-1170)
- Added a monitoring feature to evaluate the instantaneous Power ($V \cdot I$) by using eHS outputs (EFS-1101)
- Added led and RS422 port support for OP4510 standard firmware (EFSTT-68)

Bugfixes

- Fixed a bug related to eHS output average calculation that was saturating to 255 samples (EFSTT-17)
- Fixed a bug that prevent from using multiple PMSM machine blocks at the same time in the same CPU model with different parameters (EFS-1466)
- Fixed bugs in circuit parsing (SimPowerSystems workflow only) (EFSTT-37 - EFSTT-25)

Version 1.5.1

Features

- Added support for the eHSx128 form factor in the eHS Gen3 CPU block. (EFSTT-36)
- Added RT-LAB eHSx128 Gen3 example model. (EFS-775)
- Added support of circuits containing more than 72 switching elements using eHSx128 Gen3 form factor (EFSTT-3)
- Added support of circuits containing more than 32 sources using eHSx128 Gen3 form factor. (EFSTT-7)

- Updated the Analog Output Mapping and Rescaling console block to support eHSx128 Gen3. (EFS-994)
- Added error handling for 0 or infinite R, L, or C values. (EFS-998)
- Updated eHS Quickstart Guide, updated User Guide, and created OP4200 Quickstart Guide (EFS-776, EFSTT-36, EFS-775)
- Added support for PSIM and PLECS circuit models on the OP4200 platform. (EFSTT-48, EFSTT-52)
- Added support for eHS OP4200 eHS Block to automatically detect if the circuit model has changed. (EFS-925)
- Added T-type sub-module MMC (MMC5) as a separate block in the library, still maintain MMC4 product. The gating signals from CPU definition has changed.

Bugfixes

- Fixed bug with Selectable Digital Inputs not working correctly on all targets. (TT-8978)
- Fixed eHS parsing errors that could occur with certain combinations of Two-Level and/or Three-Level switches. (EFSTT-23)
- Fixed behavior of Cancel button in the OP4200 GUI for eHS. (EFS-902)
- Fixed error with the OP4200 eHS Block when the minimum eHS time-step was larger than the maximum eHS time-step. (EFS-916)
- Fixed issue in the eHS OP4200 eHS GUI related to the naming of Two-Level and Three-Level switches when placed in separate subsystems. (EFS-925)

Version 1.5.0

Features

- Added eHSx32 support on the new OPAL-RT platform: OP4200.(EFS-424)

- Introduced a new and improved GUI for eHS on OP4200 which is accessible via the Simulink library block for eHSx32 on OP4200.(EFS-424)
- Added an example project for OP4200 which consists of a boost with a two level inverter.(EFS-845)
- The Analog Output Mapping and Rescaling console block was updated to improve usability and support for future eHS form factors. (EFS-856)
- Introduced BETA version of eHSx128 form factor in eHS Gen3 CPU block. (EFS-481)
- Updated MMC training slides to include software version information and compatibility.
- Updated MMC demos to fix a display issue in MATLAB 2014b (moved the calculation units from SC_Console to SM_Subsystem).

Bugfixes

- Fixed issues related to source naming when source is contained in subsystem. This may now affect order of inputs in models build with earlier version of eFPGAsim. (TT#8968)
- Fixed an issue with glitches in the DC voltage for MMC running on a slave FPGA. (TT#8967)

Version 1.4.3

Features

- Removed the dependency to RT-XSG libraries in MMC FPGA models.(TT#8894)
- Added support for MMC models in different types of FPGAs: VC707_2, MMPK7_325T and TE0741_325T.(TT#8895)
- Added standardized SFP drive in MMC model in FPGAs V7, MMPK7_325T and TE0741_325T.(TT#8896)

- Modified MMC4 black box source code to improve the accuracy inside MMC. (TT#8897)
- Set bitstream of MMC demos in the initial files automatically using 'efsSetBitstreamFile.m'.(TT#8898)
- Added masks and documentation for the RT-XSG blocks for Dual PMSM-VDQ, Induction Machine, Angle Sensors. (TT#7638)
- Added a firmware bitstream pool directory in the Matlab path accessible by all RT-LAB models, including eFPGAsim example models. (EFS-387)
- Updated the eHS models "Two-Level Inverter" and "Three-Phase Diode Bridge" to eHSx64 Gen3 for all platforms. (EFS-395)
- Added support for SLX files for circuits designed with the SimPowerSystems and PLECS toolboxes. (EFS-402)
- Modified eHS with IOs example models to include the RT-XSG Selectable DIO blocks and . (EFS-450)
- Added support for the Loss-Compensation Algorithm for eHS for circuits designed with PLECS. (EFS-457)
- Added support for thyristors for eHS for circuits designed with PLECS. (EFS-465)
- Added support for .CCT files for circuits designed with PSIM. (EFS-488)
- Modified the eFPGAsim toolbox installer to prompt the user for administrative rights for automatic installation within the Matlab path. (EFS-511)
- The eFPGAsim JAVA packages are now installed in the Matlab static JAVA class path. (EFS-517)
- Added support for PLECS and PSIM circuit editors in the "Two-Level Inverter" and "Three-Phase Diode Bridge" example models. (EFS-537)
- Modified eHS with IOs example models to include a generic Analog Output solution (handling both the static analog outputs and the Analog Output Mapping and Rescaling function). (EFS-611)
- Added a security check in the eHS Gen3 solver to prevent the user to enter a custom solver step size outside the range available for the solver. (EFS-676)
- Added support for multiple 3-level bridges in a circuit simulated using the eHS solver. (EFS-737)
- Removed support for Xilinx ISE Design Suite for eHS with IOs example models for OP4500, OP4510 and OP5607. (EFS-761)

- Separate the library in 2 library in the library browser (eFPGAAsim and eFPGAAsim XSG). (EFS-762)
- Added an option to the eHS Gen3 CommBlk to enable an automatic communication port management that works for most firmware configurations. (EFS-763)
- Added support for three-phase measurement blocks for circuits designed with the SimPowerSystems toolbox. (EFS-764)
- Added support in eHS for circuits designed with PSIM 10.0.6. (EFS-765)

Bugfixes

- Fixed issue with MMC demos not being able to run in MATLAB 2014b. (TT#8893)
- Fixed an issue with the eHS Gen3 solver preventing the outputs to be updated when the measurement count is equal to 1, 9, 17 or 25. (TT#8768)
- Fixed an issue with the RTXSG Scope and FPGA 64-to-64 Interconnect control panels channel selection set by the block causing the selection to reset every time the Simulink model is loaded. (TT#8772)
- Fixed an issue preventing the correct switch control mapping for FPGA-based PWM Generators (TT#8812)
- Fixed an issue in the eHS Gen3 CommBlk causing the "RTE Gates" setting to reset when the model is re-opened. (TT#8814)
- Fixed an issue with the Analog Output Mapping and Rescaling Control Panel causing the last available signal not to appear in the signal selection drop-down list for each output channel. (TT#8816)
- Fixed an issue with the eHS scenarios causing all outputs to fall to zero when using a non declared scenario. (TT#8817)
- Fixed an issue with the Dual PMSM-VDQ controller block (CPU side) causing a scaling error on the Idq axis of the Ld-Lq tables while using the Standard park transform. (TT#8868)

Version 1.4.2

Features

- Support of Matlab R2015a SP1. (EFS-361)
- Removed the support of Matlab R2010b. (EFS-385)
- Support of eHSx32 Gen3 for smaller FPGA boards (OP4200 / OP5600 / OP7161). (EFS-341)
- Support of Thyristor (PSIM and SimPowerSystems circuit editors). (EFS-353)
- Support of LCA in PSIM (using the VSI block). (EFS-373)
- Support of PLECS 3.7. (TT#8732)
- Removed the support of QNX. (EFS-368)
- Beta support of PSIM 10 (requires a PSIM patch). (EFS-354)
- Implemented new VSC controller in MMC-HVDC CPU and MMC-HVDC FPGA demo models.
- Added over-current protection to MMC-HVDC FPGA and MMC-HVDC-DUO FPGA models.
- Added over-voltage protection reset function to MMC FPGA blocks in the library and 4 FPGA models.

Bugfixes

- Fixed a bug that prevents "AinDin_AdjustmentsAcquisition" block from updating properly. (TT#8733)
- Fixed a bug that caused a JAVA error while using eHS on with regional settings of Windows 7. (TT#8745)
- Fixed a bug that caused an error during parsing the switches of a PSIM circuit for a large switch number. (TT#8747)

- Fixed a bug in PMSM-SH v2 block where machine 1 dq transforms parameters were not applied properly. (TT#8746)

Version 1.4.1

Features

- Added support for RT-XSG v3.0+ in eFPGAsim, including porting the support for firmware generation using the Xilinx Vivado Suite and Matlab R2014b. (TT#8663)

- Example models "Boost and two-level bridge" and "Two-level Bridge" for eHSx64 Gen3 are provided with an OP4510 firmware, and models are configured for OP4510 by default. (TT#8656)

- Updated MMC libraries in FPGA and CPU and the files for generating bitstream for MMC4 with deadtime and overvoltage protection feature. (TT#8657)

- Added support for control of eHSx64 Gen3 inputs from another eHS core. (TT#8658)

- Corrected the eHS report log to eliminate time-step duration truncation and to fix an incorrect "Solver desired time step" value appearing the first time it is shown after the option "Provide explicit sample time for solver eHS" is unchecked. (TT#8659)

- Corrected the optimal Gs proposed by the Gs Optimization Tool is incorrect for Single-phase Three-level NPC Converter, resistive load to take into account the converter base current. (TT#8660)

- Added support for control of eHSx64 Gen3 inputs from analog inputs. (TT#8661)

- Added documentation for the Switched-Reluctance Machine (SRM) block. (TT#8632)

- Added a Quickstart Guide for the eHS solver. (TT#8662)

- Added documentation for the Analog Output Mapping and Rescaling (AOMR) block. (TT#8621)

- Added a patch to the RT-XSG blocks for the eHS solver and of the Analog Output Mapping and Rescaling function to avoid 'Bool type output port op gets indeterminate value' errors during offline simulation. (TT#8605)

- The eHSx64 Gen3 reset signal (coming from RT-LAB) is now resynchronized with the simulation step pulse (ModelSync). (TT#8664)

- Added 6 example model for the FPGA-based Modular Multilevel Converter (MMC) models to the eFPGAsim demo browser. (TT#8665)

Bugfixes

- Fixed a bug in eHSx64 gen3 that avoided the user of using more than 55 switches. (TT#8696)

- Fixed a bug in dbl2sfp function. Extended mantissa was forced to 0 in some cases leading to wrong simulation results (system time constant was reduced). (TT#8697)

- Fixed an issue causing wires to be disconnected inside one component in MMC library of eFPGAsim version v1.4.0. (TT#8636)

- Fixed an issue causing the minimum time step to set to real time step value in circuit info of the eHSx64 Gen3 block. (TT#8634)

- Fixed an issue causing Simulink not being able to change Gate controls from the Gate control selection panel. (TT#8610)

- Fixed an issue with the "Multimeter" block support causing misassignments in the measurement types and names. (TT#8666)

Version 1.4.0

Features

- Added the support of eHS Gen3 with LCA (Loss Compensation Algorithm) for 2-level and NPC converter topologies (SimPowerSystems workflow only). (TT#8594)

- Added the support of LCA in the eHS offline simulation block. (TT#8595)

- Upgraded eHS Gen2 example models to eHS Gen3 for Virtex-7 and Kintex-7 compatible chassis (NPC converter example). (TT#8596)

- Added FPGA PWMo function in the example models that can be mapped to the eHS circuit switches. (TT#7862)

- Added examples model of eHS Gen3 (3-Phase Inverter with Boost and 3-Phase inverter examples). (TT#8596)
- Added a netlist report during eHS Gen3 equation generation. (TT#8597)
- Made a tool to calculate Gs based on the topology (TT#8603)
- Added a GUI to map the gate sources to the netlist switches (eHS Gen3 only). (TT#8601)
- Increased the maximum number of scenarios available for eHS Gen3 (up to 1023). (TT#8599)
- Added the support of Matlab R2012b R2013a R2013b R2014b R2015a (32bits and 64bits). (TT#8598)
- Added a PLL and PID functions for RCP applications. (TT#8553)
- Added a new MMC topology Clamp-Double Sub-module (CDSM). It must be applied with Artemis version v7.0.2.773 and later to realize the functionalities of CDSM in a MMC system.

Bugfixes

- Fixed Unknown error a model was not including a SimPowerSystems POWERGUI or a PLECS circuit. (TT#8602)
- Fixed current measurement are wrong when the ground is present in SimPowerSystems for multi branch measurement. (TT#8504)
- Fixed the compatibility issue between the MMC block callback and RT-LAB 11.0.3. (TT#8600)

Version 0.3.8

Features

- Added example models of eHS with I/Os for OP4510, OP4500 and OP5607. (TT#8543)
- Added support of the PMSM Spatial Harmonic block v2 (Larger tables, embedded mechanical model). (TT#8545)
- Support of SRM block for Virtex-7 and Kintex7-based chassis. (TT#8544)
- Added the support of the "DC link filter + 2 inverters" mode in the inverter solver with boost block. (TT#8546)
- Added FPGA 64-to-64 Interconnect block to eFPGAsim CPU and FPGA libraries. (TT#8552)

Bugfixes

- Fixed RLC and LC component support in the eHS circuit parsing function. (TT#8555)
- Fixed NI Multisim support in eHS. (TT#8306)
- Fixed an issue in the Switched-Reluctance Motor (SRM) block that was causing an initialization error during model compilation. (TT#8557).

Version 0.3.7

Features

- Added a Neutral-Point Clamped (NPC) converter example model for eHSx16 on ML605. (TT#7612)
- Added an example model for eHSx16 with I/O interfaces for ML605. (TT#8520)
- Added a "Selectable Digital Output" block to the HIL I/O library (this block can handle static digital outputs, Event Generator signals and Pulse-Width Modulated digital outputs). Added a "Selectable Digital Input" block to the HIL I/O library (this block can handle static digital inputs, Event Detector signals and Pulse-Width Modulated digital input analysers). (TT#8521)

Bugfixes

- Fixed help link for MMC Pulse block (MMC Gate Control Panel). (TT#8440)
- Fixed an issue with eHSx64 internal sine wave generators requiring the parameters for all 32 sine wave generators to be provided (causing malfunction of the generators if the "Use as many inputs as the current netlist requires" option was selected). (TT#8517)
- Fixed eHSx16 support for mutual inductance element that was causing matrix generation to fail with error "Reference to non-existent field 'value'.". (TT#8518)
- Fixed an issue with the MMC FPGA control block to enable custom OpCtrl or OpLnk controller name. (TT#8523)
- Fixed inconsistencies in the documentation of the Analog Output Mapping and Rescaling block and Inverter Model with Boost block. (TT#7939)

Version 0.3.6

Features

- Added a MMC library that contains a block which has a choice of MMC half-bridge or full-bridge, MMC valve control blocks and 6 MMC demo models in typical Power System applications with related help files. (TT#8509)
- Support of the PMSM Spatial Harmonics solver and Inverter solver on Virtex-7 FPGAs. (TT#8508)
- Support of RL RC elements of PSIM in eHS circuit parser. (TT#8506)
- MMC 3x512: Added the option to choose whether to have faults and gates inputs or not, fixed the behavior when the selection options are unchecked. (TT#8438)
- MMC 3x512: the decimation factor can be obtained when the FPGA is in slave mode, and the following blocks are now compatible with both OP7020 and OP7000:
 - Modular Multilevel Converter with Integrated Controller (3x512 cells)
 - Modular Multilevel Converter with Integrated Controller (3x512 cells) (Valve Current and VMMC)(TT#8476)

- MMC: Fixed the bug of glitches on Vmmc when Vmmc_ave mode is checked when running MMC model with OP7000, obtained different decimation factors when there are more than one FPGA. (TT#8410)

Bugfixes

- Bugfix: "Analog Output Mapping and Rescaling block Control Panel" was not working properly when linked to the library. (TT#8507)

- Bugfix: eHSx64 initialization port number was stuck to 1 and impossible to change. (TT#8439)

- Fixed an issue in the OP7161_2-based 3x512-cell Multilevel Modular Converters (MMC) causing wrong Vmmc values in averaged mode. (TT#8425)

- Fixed incorrect sequencing of capacitor voltages received from OP7161_2-based Multilevel Modular Converters (MMC) models using the 3x512-cell MMC library. (TT#8409)

Version 0.3.5

Features

- Fix for the conversion function dbl2ssfp43.p that was returning wrong results for input values slightly inferior to powers of 2. (TT#8424)

Version 0.3.4

Features

- Added support for mutual inductances and transformers with both generations of eHS for SimPowerSystems and PSIM workflows. (TT#8420)

- Added support for eHSx64, the second generation of eHS solver. It features a higher computation power (4x), more input/outputs, better accuracy and support for scenarios. (TT#8418)
- Added support for induction machines in the motors library. (TT#8415)
- The second core of the dual eHS was assigned the same configuration and circuit as the first core. They can now be independent. (TT#8304, RT3#276253)
- Added support for the MMC model on the OP7000 generation of simulators. Also added a three-valve, 512-cells-per-valve Modular Multilevel converter block, with new implementation of MMC which removes the parameters to adjust snubber from the previous versions. (TT#8123)

Bugfixes

- Fixed the support of int32 parameters in Ansys data (TT#8417)
- Fixed an issue with the the PMSM SH solver core. The Current results were $\sqrt{2/3}$ off the reference results when using the Ansys machine data. (TT#8416)
- Bugfix: the CPU block was keeping the last solver output state when reset. When reset, the solver is outputting 0 on all outputs now. (TT#8371)

Version 0.3.3

Features

- Added entry for DeltaT/C in the documentation of the Capacitor Differential Equation Solver block. (TT#8283)
- Support of parasitic parallel resistance in the boost inductor (dual inverter with boost block). (TT#8183)
- Add Ansys support in PMSM Solver Spatial Harmonics (TT#8182)
- Support of OP4500/VC707 for motors/converters/IOs/Sensors blocks (TT#8181)

Bugfixes

- Fixed an issue where the Vmmc value would drop by 16 volts when switching to normal mode. (TT#8124)

Version 0.3.2

Features

- The "2 DC source + 2 Inverters" mode of the Inverter_Solver_wboost block is not supported and returns an appropriate Matlab error to the user. (TT#8111)

- NaN were inserted in the Ld Lq and flux tables when the breakpoints were not the same for Id and Iq or the breakpoints were not defined for +/- max lamp value (symmetric around 0). NaN are now replaced by the nearest non-NaN value. (TT#8105)

- The eHS configuration matrix location is now provided with its relative path, enabling the packaging and distribution of pre-compiled RT-LAB projects with the eHS feature. (TT#8076)

- Add support for FPGA based MMC valve and valve control. Requires RT-LAB v10.7.3 or later. (TT#7743)

- Added a 512-cell Modular Multilevel Converter (MMC) Valve and Valve Controller models. Requires RT-LAB v10.7.3 or later. (TT#7743)

- Added the RT-XSG Scope to the eFPGAsim I/O library. This scope enables the monitoring of internal FPGA signals with very fine time resolution (down to 5 ns). (TT#7482)

Version 0.3.1

Features

- In machine models PMSM-VDQ and PMSM-SH, the Rabc force feature did not operate properly. The equation has been fixed. (TT#8055)
- Added the RT-XSG block for the "Analog Output Mapping and Rescaling" function. (TT#7882)
- Added support for initial states of Capacitor and Inductor in eHS for PLECS. (TT#7880)

Bugfixes

- Fixed an issue in the PMSM-SH machine model related to a 30-step delay between motor 1 and 2 computation not being accepted by the callback despite its being a legal setting. (TT#8054)
- Fixed an issue in the PMSM-SH machine model related to the FPGA interpolation function malfunction causing spikes on the torque. (TT#8053)
- Fixed an issue in the PMSM-VDQ machine: the block did not update properly when motor 2 is used in LdLq table mode. (TT#8052)
- Fixed an issue in the PMSM-VDQ machine model where the flux and back emf amplitude were not right when the user set the LdLq table mode. (TT#8051)
- Fixed an issue with the allocation of communication port numbers of the Dual eHS block when the linked OpCtrl block was taken from the Opal-RT I/O Common library. (TT#8005)

Version 0.3.0

Features

- Added support for nonzero capacitor initial voltage and inductor initial current in eHS. (TT#7880)
- Added support OP4500 Kintex7-based hardware platform for the eHS solver. (TT#7898)

- Added support for switch control polarity selection (active-high or active-low) in eHS. (TT#7881)
- Added support for AC and DC voltage and current sources in eHS, implemented as embedded source signal generators on the FPGA entity of eHS. (TT#7879)
- Added a very low leakage capacitor model block in the eFPGAsim Elements libraries. (TT#7878)

Version 0.2.4

Features

- Added the 2-Level Inverter with Boost block. (TT#8031)
- Added support for OP7020 and OP5607 Virtex7-based hardware platform for the eHS solver and Dual PMSM-VDQ motor model. (TT#7900)

Improved Documentation and Error Reporting

- Enhanced the eHS solver RT-XSG block packaging and documentation. (TT#7899)

Version 0.2.3

Features

- Added a 24-phase PMSM motor function. (TT#8032)

Version 0.2.2

Features

- Added support for OpLnk controller blocks (in addition to OpCtrl's) for the eHS solver. (TT#7815)

Version 0.2.1

Features

- Added support for PLECS to design the circuits used by the eHS solver. (TT#7759)

- Added the "pulse selection" parameter in the eHS2 solver (a.k.a. "from Din"). (TT#7622)

Version 0.2.0

Features

- Modification of PMSM example model. Links with RT-XSG are now broken. Model can run off-line without RT-XSG installed. (TT#6719)

Bugfixes

- Fixed strange behavior of PMSM torque in motor model. (TT#6749)

- Fixed problem of signal routing when compiling models with 2 motors. (TT#6725)

RT-XSG for Vivado

Version 3.3.0

Features

- DataLogger.

Version 3.2.10

Bugfixes

- Aurora block had a wrong parameter's value.
- OP5342 timing for all FPGAs.
- Compatibility with R2016b.

Version 3.2.9

Features

- HCIG: IEC60044-8 support.

Bugfixes

- Bitstream's generation: constraints application fix (FPGATT-595) and error reporting (FPGATT-592).

- OP5342 at 2.000 MSPS in OP4200 with CPU at 1 GHz and FPGA at 200 MHz (FPGA-427). It was 1.98 MSPS.
- DOV: Enabled the resize of the configuration window (FPGATT-369).

Deprecation and Removals

- Removed support of Matlab R2014b, R2015a/b, R2016a.
- Removed support of Xilinx Vivado 2015.3, 2015.4 and all 2016.

Version 3.2.8

Features

- SPI block support
- OP5367, 16 Digital IN with programmable threshold and 16 digital OUT support for OP4510 only
- OP5334, 16 analog OUT 2 MSPS non-isolated beta support for OP5650, OP5707, OP4510 and OP4200
- HCIG update with Time Stamp Bridge (TSB) support
- Vivado 2019.2 with MathWorks Matlab 2019a and 2019b BETA support
- Obsolescence warning on Vivado prior to 2017.1 with Matlab prior to 2016b starting from the next RT-XSG revision

Bugfixes

- OP5143/Artix-7 timing closure improvement

- MuSE remote crash detection bug fix for all systems

Version 3.2.7

Features

- Improvement by providing designer help by warning the DataIN/OUT blocks configurations without FIFO use (FPGA-345)
- Added protection in user interface of DataIn/DataOut blocks to warn the user to use FIFO mode when the blocks are connected to analog I/O blocks (FPGA-345, 346)

Bugfixes

- OP7000 V2 - Primary FPGA (OP7170_1) - bug fix on Analog OUT outputting 0V when Default Output Value (DOV) is activated and when the OP7000 is in slave mode (OP7000NG-491)
- OP7000 V2 - Primary FPGA (OP7170_1) - bug fix on synchronization signaling when the OP7000 is connected to a second OPAL-RT unit in slave mode (OP7000NG-484)
- Correction on OP5332 netlist for OP5#07 only. (FPGATT-318)

Version 3.2.6

Features

- Added Default Output Value support during Pause and Reset simulation states, set by default to 0V, but is modifiable from the Hardware Configuration panel for each channel.
- Support for OP7000 V2 Primary FPGA board (OP7170-1) with Kintex-7 FPGA (XC7K410T-2FFG900).

- New Architecture Type "No MuSE" for freeing up FPGA resource for OP4510/325T, OP4510/410T and OP5#07. This option is accessible via the Architecture Type parameter of the Synthesis Manager block.
- Vivado 2018.3/Matlab 2018a support.
- Vivado 2019.1/Matlab 2018b support.

Bugfixes

- HCIG update with Resolver support. (FPGATT-203)

Version 3.2.5

Features

- Increased maximum number of CPU-FPGA DataIn/DataOut communication ports to 64. This modification is available for all platforms but OP4200.
- Added support for new OP7000 Primary FPGA board (OP7170-1) with Kintex-7 FPGA (XC7K410T-2FFG900). This support is in BETA mode. (OP7000NG-215)
- Added support for new OP5367 TypeB mezzanine module with 16 DIN with programmable threshold and 16 DOUT. The module is presently supported on OP4510 only.

Bugfixes

- Added option for endianness control for Generic Aurora communication. (FPGATT-312)
- Fixed problem when loading EEPROM gain and offset values for OP5332 when running at 200 MHz, which caused undesired negative output glitches on some channels. (FPGATT-318)

- Fixed issue in I2C sequencer that prevented the proper output of the hardware synchronization pulse on the OP5650 (Artix-7) platform. (FPGATT-334)

Version 3.2.4 (Restricted Release)

Features

- Added RT-XSG model examples, particularly for the OP5650.

Bugfixes

- Mezzanine and FPGA's carrier list correction by showing at the top the value "empty". (FPGATT-263)
- RT-XSG multi-rate support correction (decimation different than the user clock period that needs to implement clock enable logic by Vivado). (FPGATT-288)
- Updated the HCIG for the RT-XSG schematic support of Goto/From and bus selector blocks.
- MuSE updated with more larger DMA transfer size > 64 KB and improved the synchronization with time out when the remote doesn't respond (i.e. is not a real MuSE remote).

Version 3.2.3

Features

- OP5600/OP5143 (Artix 7) with MuSE support (without eHS). (FPGATT-266)
- Polymorphism enable register for software / driver control on important information to be redirected to the user.

Bugfixes

- Multi-voltage range support corrections.

Version 3.2.2

Features

- Multi user System Expansion (MuSE) with embedded synchronization logic for OP5#07, OP45#0 and OP4200 (Remote only).
- MuSE Advanced Synchronization improvements (output synchronization alignment between OPAL-RT simulator units using Central and Remote roles). (IOSFP-555, 557, 572)
- OP5600/OP5143 (Artix 7) improvements without eHS and without full MuSE support
- Signal Integrity constraint support improvements (drive strength and slew rate constraint support with mezzanine's slot and channel resolution)
- RT-XSG model standardization with new OPAL-RT Polymorphism feature support: grouping IO boards having same functionality, some cross-compatibility look up table on hardware identifiers. (BIS-52, 53)
- Hardware Configuration and Interconnection Generation improvements. (HCIG; .conf/.opal) (FPGATT-228, 229, 249, FPGA-80, 220)

Improved Documentation and Error Reporting

- Addition of design examples for learning the optical communication using the OP4510 with its MGT/SFP using the Xilinx Aurora IP CORE. (FPGA-114)

Version 3.2.1 (Restricted Release)

Features

- Integration of an option to use advanced Xilinx pre-defined parameters for the sub-tools (Tcl commands as "opt_design, map_design, route_design") for increasing the probability of achieving timing closure for tight design/FPGA.
- Multi User System Expansion (MuSE) with flash update support.
- Matlab 2018A support for Vivado 2018.2.
- Vivado 2018.2 support.
- Vivado 2018.1 support.
- New FPGA Artix 7 support (xc7a200tfg676-3) for OP5600/OP5143 product with 8 mezzanines (no MuSE).
- User clock set to 200 MHz when eHS is detected. (FPGATT-143)
- Implementation of a power down sequence with 7 Series GTX/GTP design for avoiding PCIe loss with VC707. (<https://www.xilinx.com/support/answers/59294.html> ; FPGATT-130)
- Hardware Configuration and Interconnection Generation improvements. (HCIG; .conf/.opal) (FPGATT-102; FPGATT-183)
- IO Block configuration and name's logic verification improvements. (FPGATT-106/140)
- MuSE - Prevent user from generating a remote bitstream containing eHS block. (IOSFP-349)

Bugfixes

- Script correction for terminating the bitstream generation for the OP4200 with correct name. (FPGATT-165; FPGATT-178)

Version 3.2.0 (Restricted Release)

Features

- Added support for High Speed Link (HSL) for 4 first MGT ports for OP5#707 (the limitation of 4 MGTs is the total of Aurora and HSL). HSL is supported for any port for other product. There is no flash update for remote units.
- Implemented logic to detect eHS block and pops out warning to use 200 MHz if not set. (FPGATT-143)

Bugfixes

- Hardware Configuration and Interconnection Generation (HCIG) bug fixes. (RTXSG-49, RTXSG-68, FPGATT-97)

Deprecation and Removals

- Removed support of MMPK7 (OP4500), end of life.

Version 3.1.10

Bugfixes

- Correction on a bug when changing the hardware configuration. A modification on script opxsgIOBlockUpdate was made to improve the verification of assigned hardware in the model, but the type of the returned value for mezzanine string change whether opening the model or it is already open.

Version 3.1.9

Features

- OP5607/OP5707 rev.3 support.
- Reinforced OP5342 reset circuitry for removing metastability that might stall the I2C sequencer.
- Applying drive specific strengths for OP5352 and OP5360-2 in Virtex7, Kintex7 and Zynq based systems. (PF317500-6 and PF617539-7)
- Support of the user clock of 200 MHz for the conversion's trigger in the 40 MHz architecture of OP5332. (FPGATT-124)
- Xilinx Vivado 2017.3 and 2017.4 support improvements. (FPGA-78, FPGATT-33, FPGATT-139)
- Support of BiSS-C BETA
- Support of SSI BETA
- Message and configuration improvements - Path length's verification: Not applied to Windows 10 systems. (FPGA-139 and FPGATT-33).

Bugfixes

- Hardware Configuration and Interconnection Generation (HCIG) bug fixes. (FPGATT-97, FPGATT-127)

Version 3.1.8

Features

- Added support for Xilinx Vivado 2017.3 and 2017.4 support with Mathworks Matlab R2017b.
- Added OP5332 (analog OUT @ 2 MSPS) support, added new constraints for OP5342 (Analog IN @ 2 MSPS) and added new clocking domain (64 MHz) for the OP5#07 systems.
- Updated the I2C Sequencer for reading the new IDs of the 126-0308 rev.4.0. Added register address 0x22018.
- EnDat 2.2 bug fixes: Modified the EnDat Master Interface "Ready" manager. Now in VHDL, uses the EC_STATE signal from ENDATREDUCED.
- EnDat 2.2 Master: Added features to prevent the trigger of a EnDat transaction if the previous transaction is not finished or if the bus speed requested "Freq_OEM" is 0 (illegal) or 1 (16 MHz).
- Updated sample RT-LAB models that guides RT-XSG models (buses BusSelector and BusCreator). (RTXSG-63)
- RT-XSG block improvement - Auto-assign 'Direction' to 'Both' when an 'ExpansionSignal' card's 'Type' is selected. (FPGATT-47)
- Synthesis Manager block and Expansion signal block improvements (clock period refresh and direction assignment). (FPGATT-84, FPGATT-47)

Bugfixes

- HCIG (Hardware Configuration and Interconnection Generation scripts) bug fixes and updated documentation (auto .conf and .opal generation). (FPGATT-83, FPGATT-89, RTXSG-62)
- OP4200 Zynq @667 MHz (V.1.) and @ 1 GHz (V.2.) Gray Zone selection bug fixes. (FPGATT-81)

Improved Documentation and Error Reporting

- Message and configuration improvements - Correction on error message display for SynthesisManager when updating block; user clock refreshing function. (FPGATT-78, FPGATT-18)

Version 3.1.7

Features

- Added OP5332 support for the OP4510. Updated the Gray Zone with additional clocks and new MMCM port association and updated the interrelated timing constraints. Updated the Version block with additional clocks in the Synthesis Manager block (rtxsg_tools.slx).
- Enforced support for AOMR. Partial support for eHS. Script corrections in nodeToSubsystem.m. Updated script startPoint_tracebackSignal.m : prints the config file's name generated. Modified get_confBlockInfo.m & create_opal_file.m: major modifications for support of AOMR and eHS.
- Added support of EnDat 2.2 rotative protocol communication (Master and Slave).
- OP4200: Added support for Zynq 1 GHz.
- Encoder Out: A parameter is added for the Z pulse width. It sets the width of the Z pulse slice block under the mask. Encoder Output: New "Synchronization pulse width" added to the documentation. (FPGATT-64)
- Synthesis Manager block: enlarged the FPGA Development board dialog box.
- Added support Vivado 2017.2 and Matlab 2016B and 2017A.

Bugfixes

- Made correction in the rtxsg_tools.slx for being visible in Simulink browser RT-XSG/Tools. (FPGATT-59)
- Fixed the error of emcclk when arrive write_bitstream process for OP4500 with Vivado 2016.3. (FPGATT-65)
- Fixed deadlock on TX_READY signal (TX_READY always stays at zero after a fifo full). (FPGATT-72)

Version 3.1.6

Features

- Added support of RS485 TypeB Mezzanine(OP5368) for the OP4510 and OP5707 systems.
- Vivado 2017.1 and Matlab R2016A support.
- OP5342 full support for OP4510 and OP4200, restricted support for OP5#07 (specific customer only).
- Added Hardware Configuration and Interconnections Generation (HCIG) algorithm's scripts and documentation. (GFDB-##)
- An opVerifyAuroraBlockparams.m is a new script for gathering all Generic Aurora Blocks in a model and proceed to a verification off these parameters: MGT Reset Input use, MGT reference clock (for same MGT Quad), MGT Line rate (or same MGT Quad). (RTXSG-40)

Bugfixes

- Fix the problem of incoherence in the selection of the FPGA between the Synthesis block and the Hardware Configuration block (RTXSG-37)

Version 3.1.5

Features

- Added a parallelizer and a serializer blocks. (FPGATT-51)
- OP5342 support for the OP5607 / OP5707 with 1 MSPS limitation: new timing constraints (slot's granularity).

- Update Synthesis Manager Block: Before setting the interface block parameters, the CarrierName parameter (from the HardwareConfig block) must be verified and updated if necessary.(FPGATT-34)
- New Synthesis Manager Block: merge Version, Hardware and Synthesis Blocks in the same block (SynthesisManager). This new feature automatically updates older models with the new block.
- Resynchronisation software: "Update Requests" generation support and overrun's notification (data transfer even if overrun).
- Update block "Register max fanout": was using efsDisplayCb from eFPGAsim, changed to xsgDisplayCb.
- Update IO Block GUI: Verify if IO blocks need to be updated/reconfigured after the hardware change in the Hardware Config Block.

Bugfixes

- Fixed an issue with the default IPCache and Partition values in the new SynthesisManager block
- Fixed an issue caused an error when checking the path oh the model
- Matlab R2015B support. Correction in opxsgGetBitstreamVersion.m. (RTXSG-29)

Improved Documentation and Error Reporting

- OPAL_RT_VivadoPathCheck for informing through a warning message that some characters in the Vivado temporary path could be harmful.

Version 3.1.4

Features

- Register-Correction of reading the Alpha ID in the RTXSG version and changing the encoding.
- MGT/SFP-Added a delay on o_SDA and on o_Z for respecting the I2C specification hold timing of 100 ns for the Si5338 clock generator (clock reference).
- OP5342-Added support of an analog input mezzanine "OP5342" @ maximum 2 MSPS (but maximum 1 MSPS for OP5#07).
- MATLAB Function-MCode function to serialize words to the Aurora AXI interface (soft/Simulink/libRxx/m/opxsgGenericAuroraSender.m).

Bugfixes

- Vivado and Windows 7-Apply a workaround to fix problem with 260 characters limitations for PATH in Windows. The problem occurs mostly when Sysgen is generating and synthesizing IP cores.

Improved Documentation and Error Reporting

- Error Management - Added function of reporting errors (with file location and line number information; soft/Simulink/libRxx/m/CatchErrorReporter.m).

Version 3.1.3

Features

- Vivado: Added support of Vivado 2015.4 by taking into account the Xilinx Compilation type "Synthesized_Checkpoint".
- OP4200: Added support of User LEDs.

- Vivado: Added support of 2016.3 (added synth_stub option in Tcl script for generating the user model stub) with IP Cache option available for better Synthesis time achievement.
- VC707: Updated the Gray Zone by adding dont_touch attribute on configuration clock for generating a bitstream.
- OP4200 and Vivado 2016.3: Changed a constraint for allowing the generation of a bitstream (SPIx1).
- Added support of Vivado 2016.4.
- Updated the Selectable DIO block (specific to the TSDIO functionality) by adding a delay before the Model Synchronization pulse. (TT#8978)
- Mezzanine OP5342: Added support of the new Analog IN at 2 MSPS for OP4510 and OP5607 with Signal Integrity control (IO's drive strength specific modifications; additional timing constraints).
- Mezzanine OP5342: Bring correction on safe frequency support of the I2C communication bus under the user clock following (100 or 200 MHz).
- Selectable DIO: added synchronization on ModelSync for Selectable DO (rtxsg_application_lib.slx).

Bugfixes

- OP4510: Fixed issue with Expansion slot IO Block configuration (ExpansionSignal type). (TT#8969)

Improved Documentation and Error Reporting

- Added new report as hardware configuration file (Product, FPGA, mezzanine names) in the project folder (hw_config.txt).

Version 3.1.2

Features

- Add an option to enable or disable the CRC in the Generic Aurora. (TT#8951)
- Added support for new IO carrier names of the OP4200 system. (TT#)
- Added feature to generate the update request internally for OP4500. (TT8937#)

Bugfixes

- Fixed One step delay in Generic Aurora transmission when one word is transmitted per time step. (TT#8839)
- Fixed fatal exception again Matlab 2015aSP1. (TT8888#)
- Modify design to prevent flipping board index problem on OP4510 system. (TT8938#)

Version 3.1.1

Features

- Added mask for XSG blackbox resynch_fanout10_ff (register with MAX_FANOUT) attribute. The existing way to instantiate this blackbox manually in the designs has the disadvantage that the value of the MAX_FANOUT attribute is the same across all instances of this blackbox. By using this mask the value of the attribute can be changed with a mask parameter. (TT#8556)
- Added support for Board Index > 31 for the OP5607 (VC707). (TT#8748)

Bugfixes

- Fixed Mask Visibility of PWMO block When option "As Block Parameter" is chosen for InitPhase. (TT#8829)

Version 3.1.0

Features

- Added a "Selectable DIO" functionality in RT-XSG. (TT#8791)
- Added support for Matlab 2015aSP1. (TT#8607)
- Added support for OP4200 (Zynq 7030) (alpha release). (TT#8741)
- Added support for OP5363 mezzanine (32 DI High Impedance) for Virtex-7 (OP5700, OP5607), and Kintex-7 (OP4510,OP4520). (TT#8369)
- Added a mechanism to detect a model crash in Hypersim, so that a protection logic can be implemented for the outputs of the simulator. (TT#8739)
- Added a protection to prevent endless error reporting when performing an update diagram (Ctrl-D) on a model when the Version block name is not exactly 'Version'. (TT#8757)
- Replaced the feature "open timing analyzer" by a timing text-file report. (TT#8623)

Bugfixes

- Fixed SineCosine block obsolescence in Common/op_csin block with interpolated-LUT-based sine wave generator. (TT#4472)
- Fixed Park/Inversed Park transform blocks with updated Common/op_csin block. (TT#8576, RT3#284360)
- Fixed an issue preventing the support of space characters in the model path. (TT#8622)

- Fixed an issue causing timing violation errors when generating bitstreams for OP4500. (TT#8783)

- Fixed an issue with chassis ID value changing from 0 to 31 after bitstream is programmed on systems with Virtex7 FPGA. (TT#8793)

Version 3.0.0

Features

- Added an option in the Version block to force the maximum fanout value for the ModelSync and nRst signals. (TT#8556)

- Improved PCIe timing management for Kintex7 FPGA (MMPK7 and TE0741) by relaxing maxskew parameter. (TT#8503)

Bugfixes

- Fixed filtering of input signals for TSDI and PWMI operating at 200MHz. (TT#8573)

- Fixed Generic Aurora Communication block to prevent Matlab crash at model opening. (TT#8505)

MMC

Version 2.2.0

Features

- Added new demo of VSC switching function -- TSB AC/AC Converter in CPU.
- Added new demo of MMC HVDC in CPU, it combines MMC CPU detailed model and average model in one demo.
- Added MMC RT-XSG model for the demo bitstream.

Version 2.1.0

Features

- Support for new Matlab versions. Add support of Matlab 2019a and Matlab 2019b.

Version 2.0.0

Features

- Support for new Matlab versions. The official list is now 2015b, 2016a, 2016b, 2017a, 2017b, 2018a and 2018b.
- Support Sub-module states transmission in new protocol in MMC FPGA models. Please note in this version no protocol communication is supported in OP4510.

Bugfixes

- Version of MMC showing in Matlab command window when the command 'ver' is given.
- Reworked the libraries displayed in the Simulink Library Browser.
- Updated MMC unitary test procedure.
- Added documentation for RT-XSG blocks which are inside MMC library.
- Fixed the bug that MMC demos cannot be compiled on windows target.
- Added all MMC examples in RTLAB New Project wizard (supported with RTLAB 2019.3 and above).

Deprecation and Removals

- Dropped support of the following Matlab versions: 2011b, 2012b, 2013b and 2014b.

Version 1.0.0

Features

- MMC6 Hybrid MMC models in FPGA are available. The MMC can have up to three type of SM (e.g. Half bridge sub-module (HBSM), Full bridge sub-module (FBSM), Clamped double sub-module (CDSM), or T-Type sub-module) in one valve.
- MMC6 Hybrid MMC RT-XSG model and bitstream compilation are only available in Xilinx Vivado.
- This MMC version supports FPGA types OP7020, OP5607 and OP4510.
- Software Artemis 7.2.1 and upper, RTLAB 11.2.1 and upper and RT-EVENT are needed to run MMC demos.
- This MMC version supports Matlab 2011b, 2012b, 2014b, 2015b and 2016b.

